



TITLE: Adaptive Radio Transceiver With
Polyphase Calibration
INVENTOR: Stephen Wu et al.
APPLICATION NO.: 09/692,654,
CONF. NO. 7167; DOCKET NO. 15266US01
ATTORNEY: M.T.Cruz, PHONE: 312-775-8000

FIG. 1

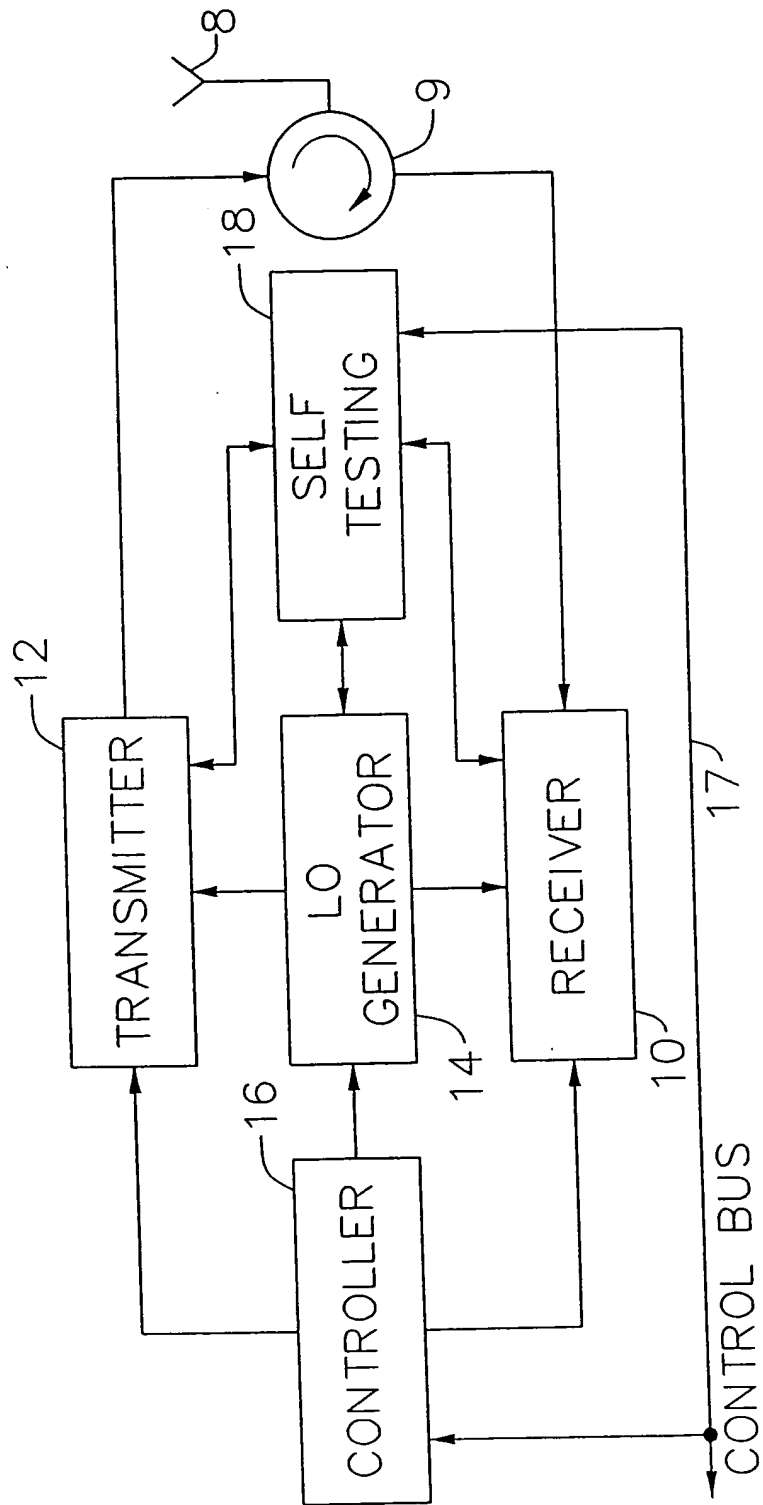




FIG. 2

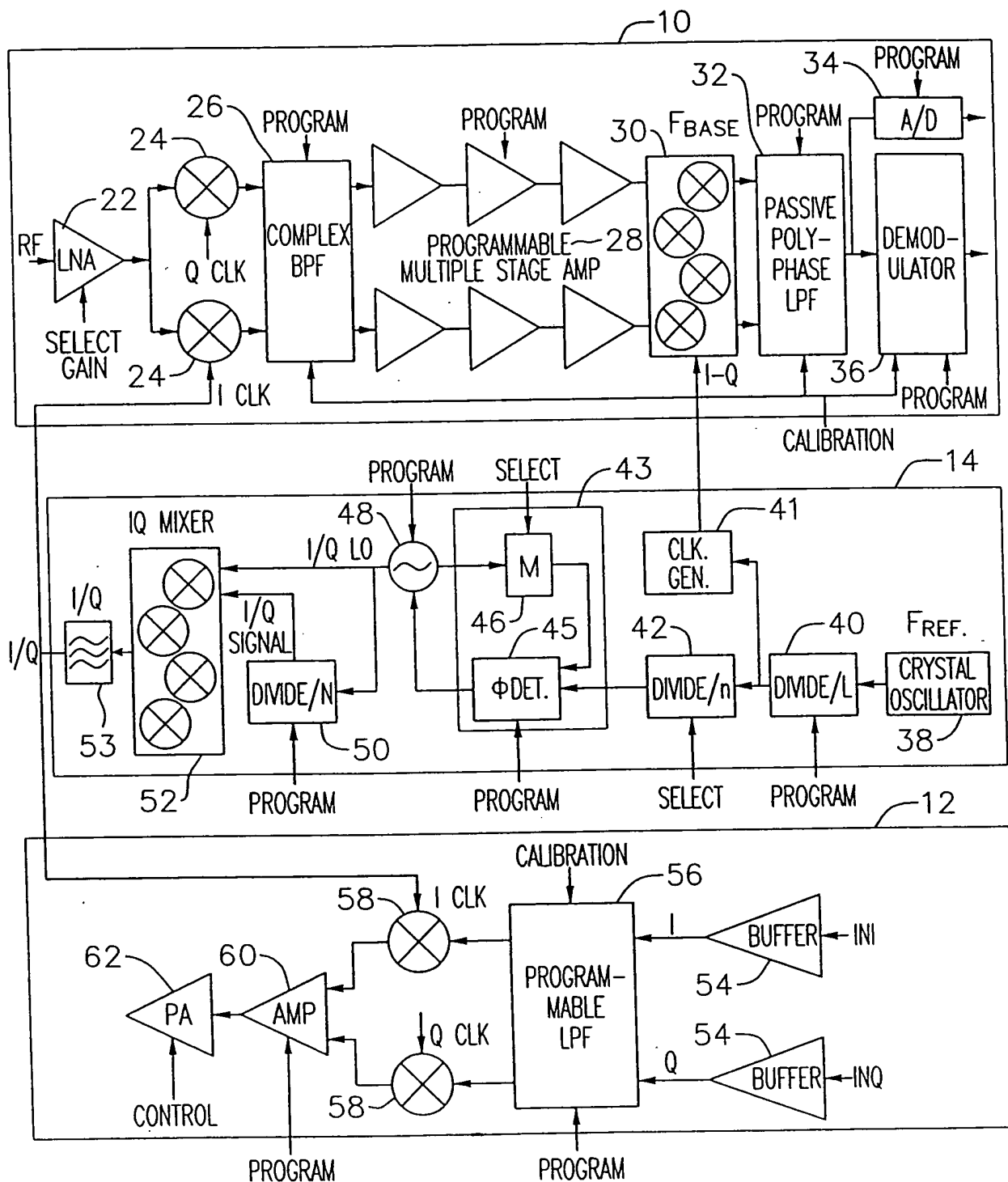




FIG. 3

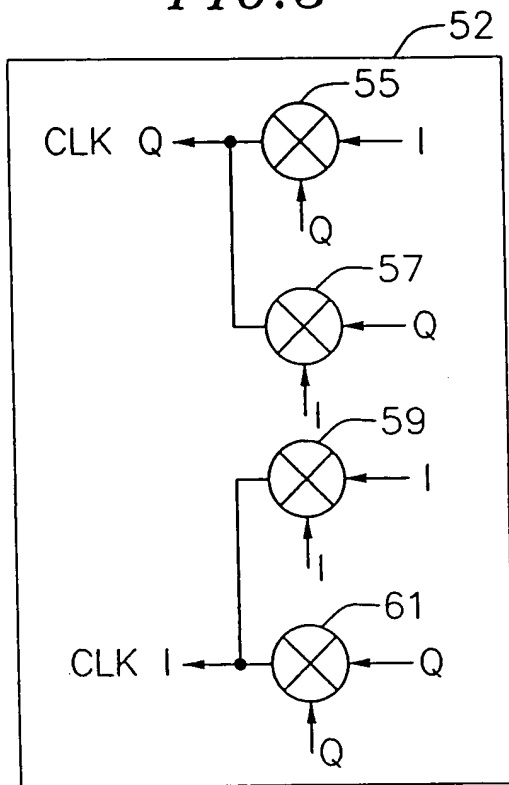
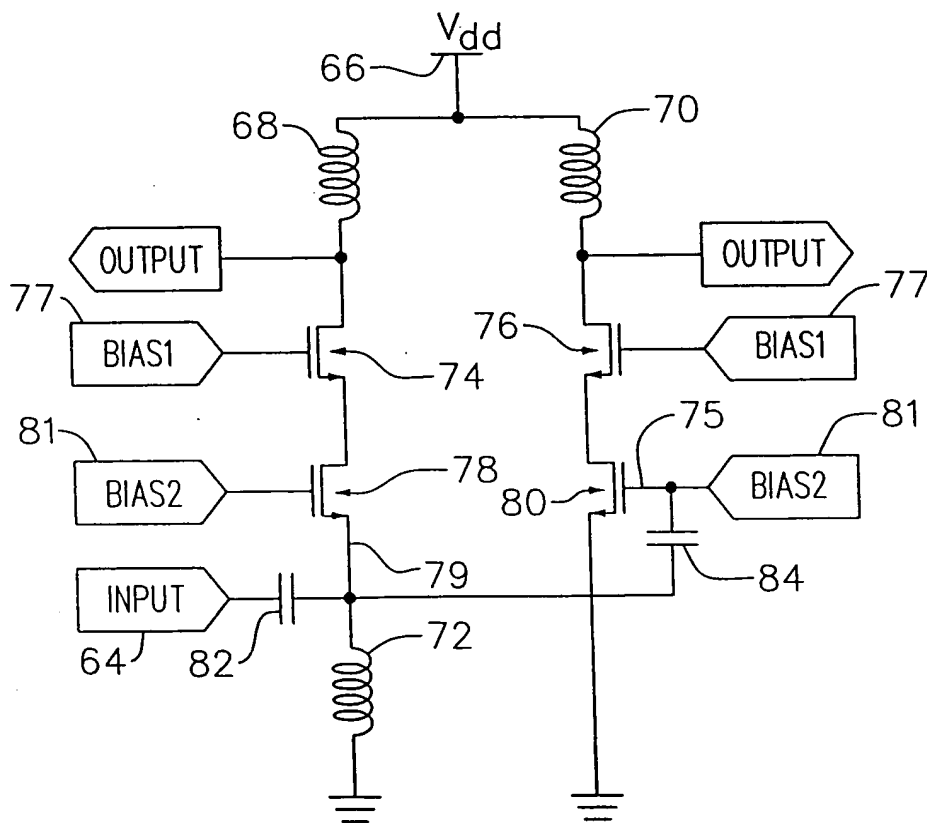


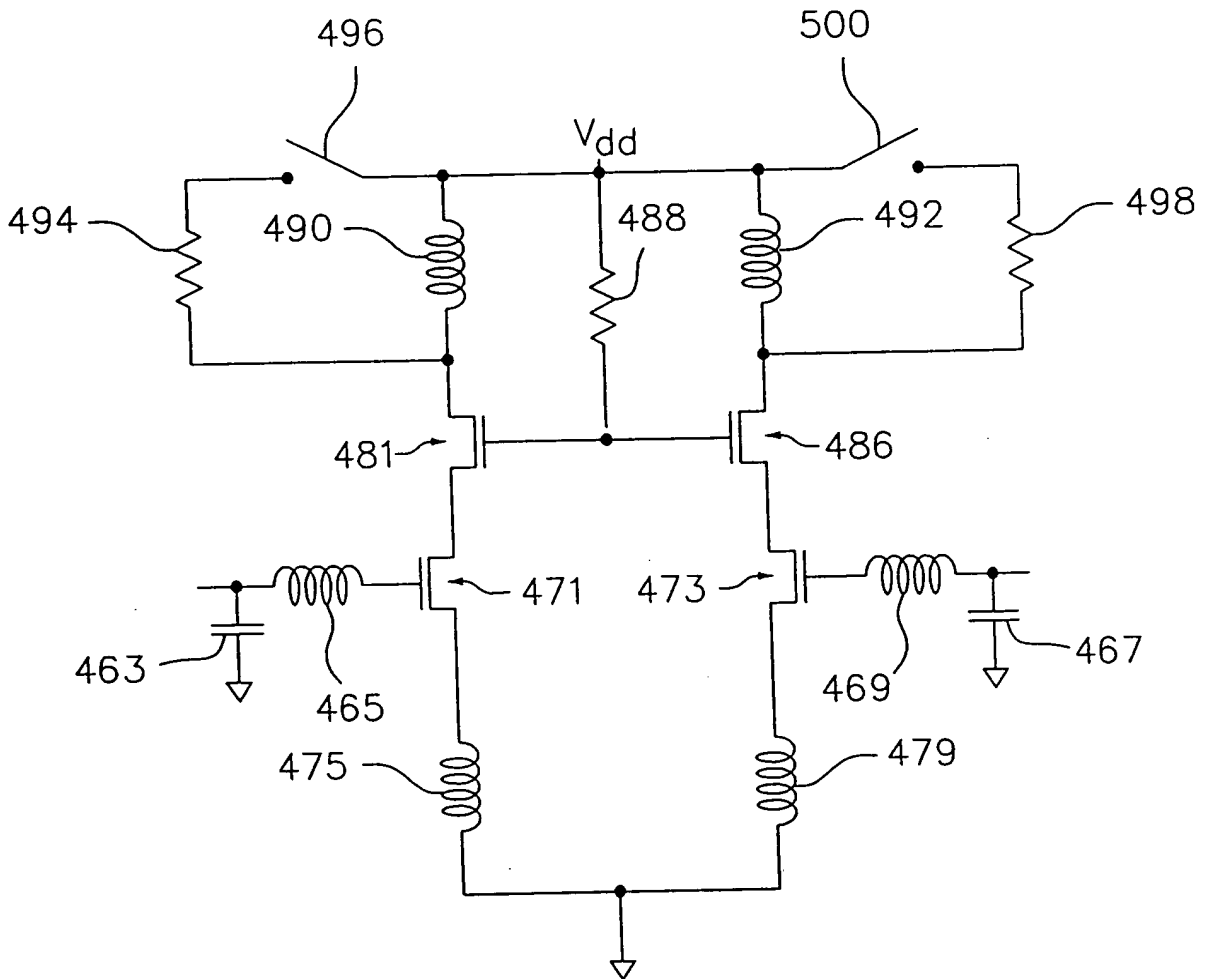
FIG. 4

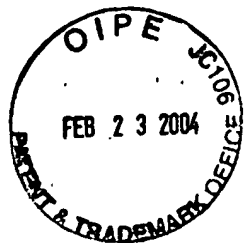




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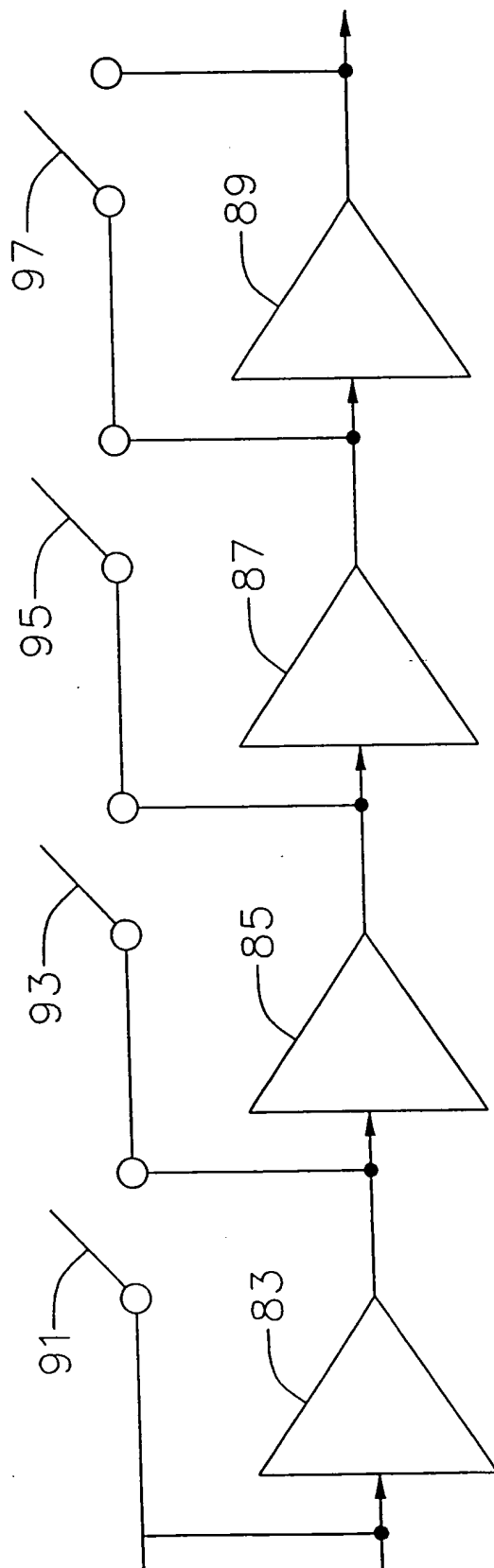
FIG. 4(a)





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FIG. 5



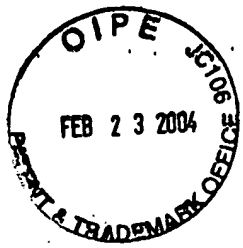
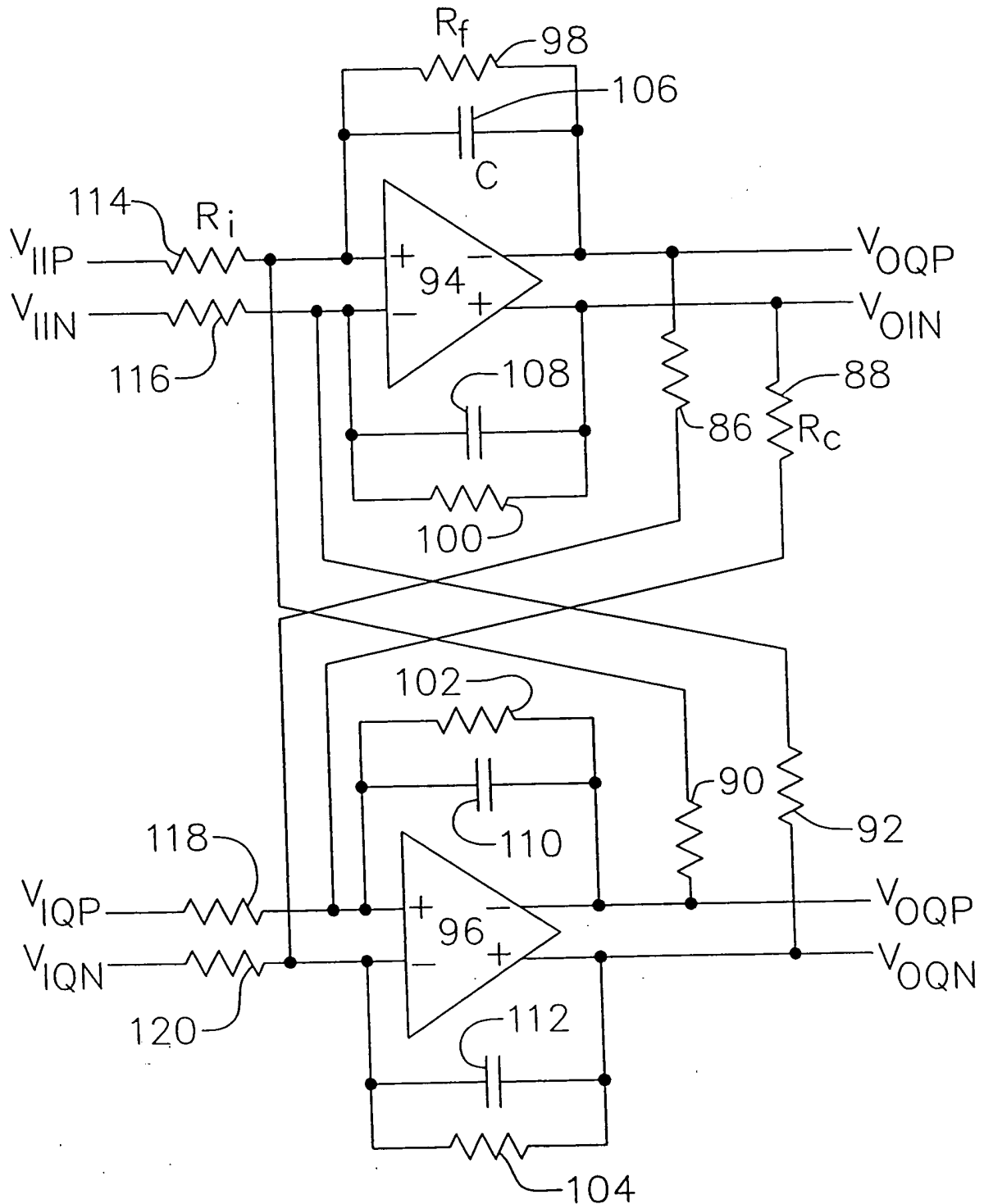


FIG. 6



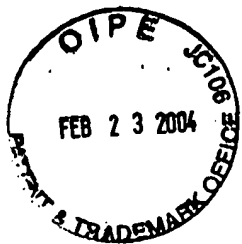


FIG. 7

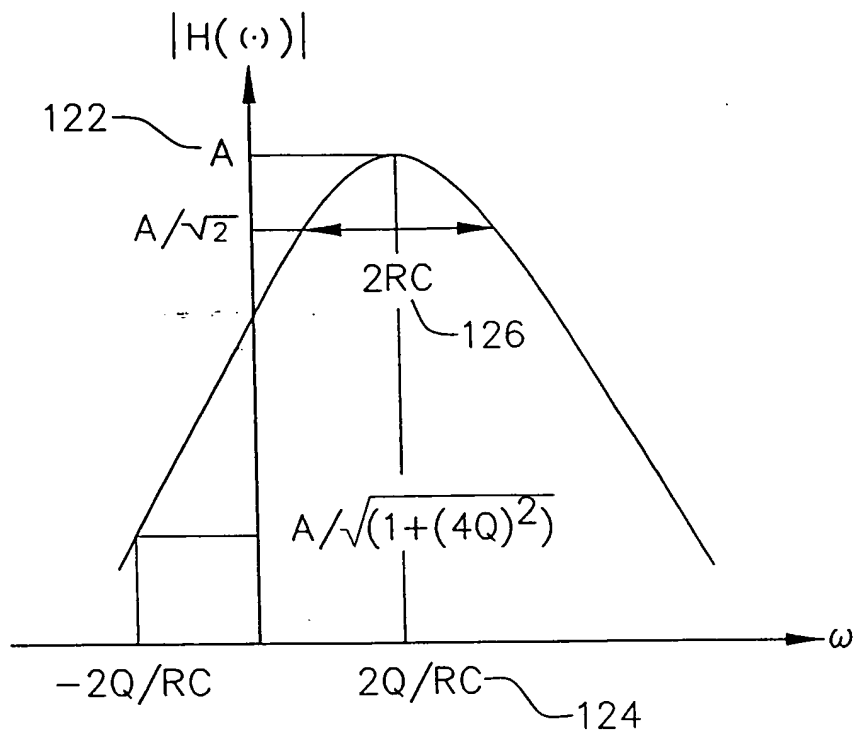


FIG. 8

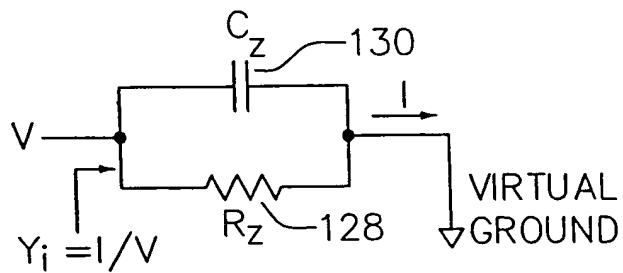
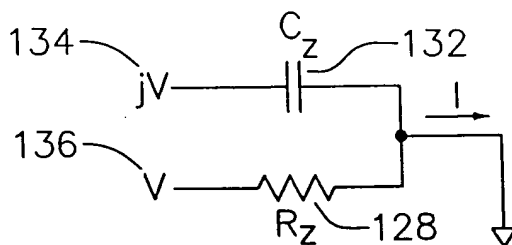


FIG. 9



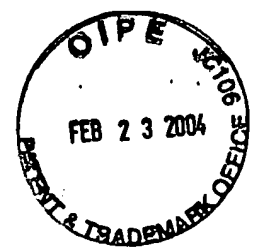
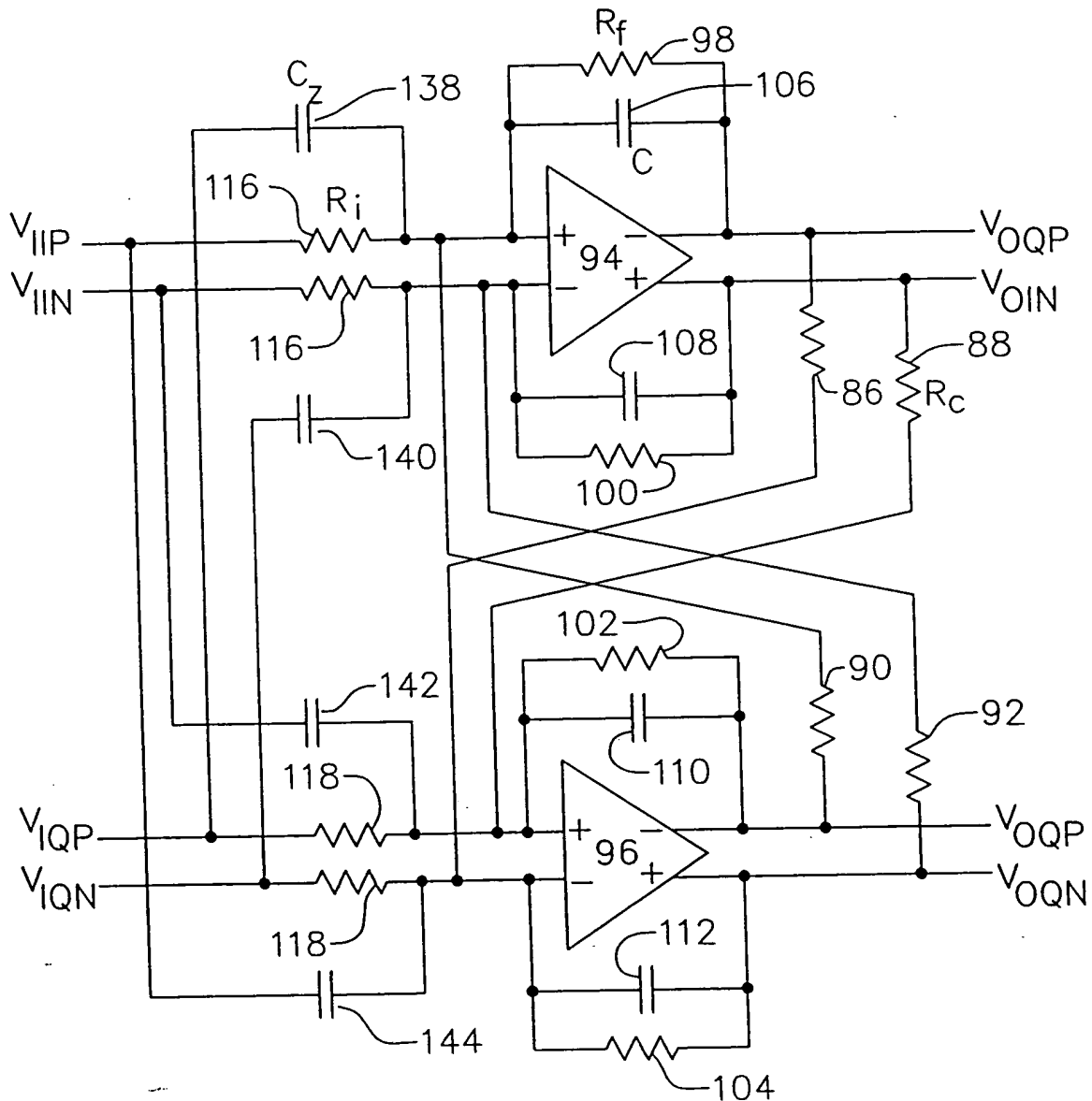


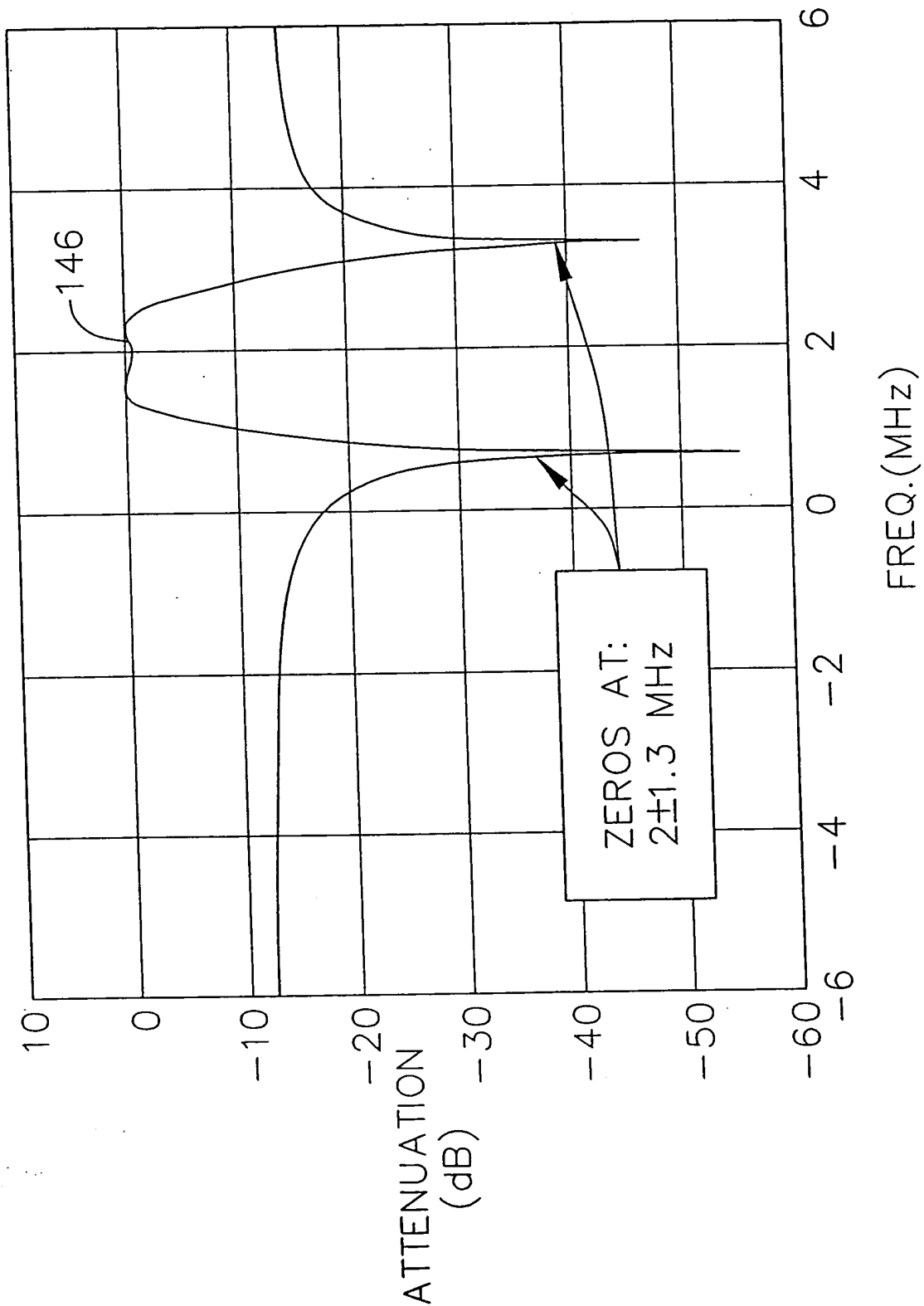
FIG. 10

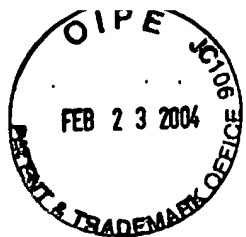




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FIG. 11





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FIG. 12(a)

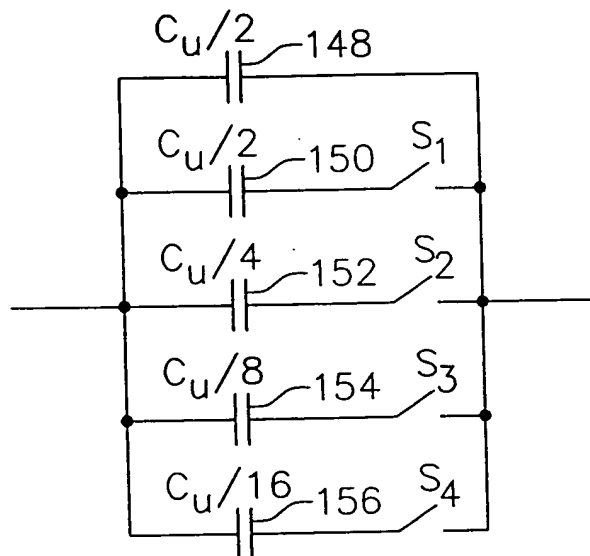
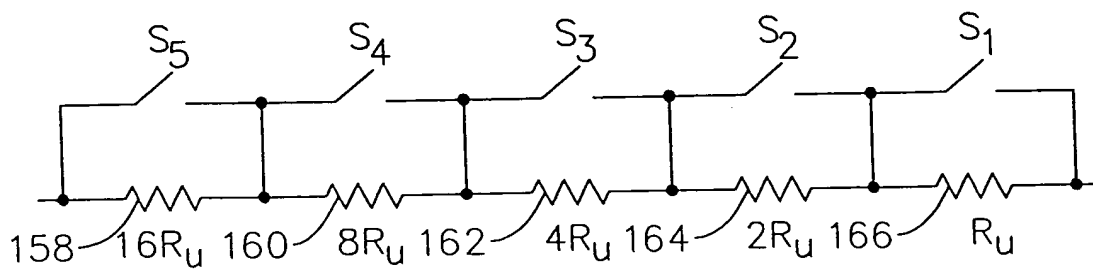


FIG. 12(b)



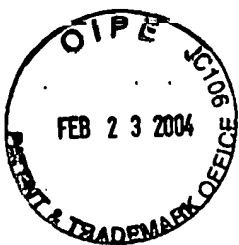


FIG. 13

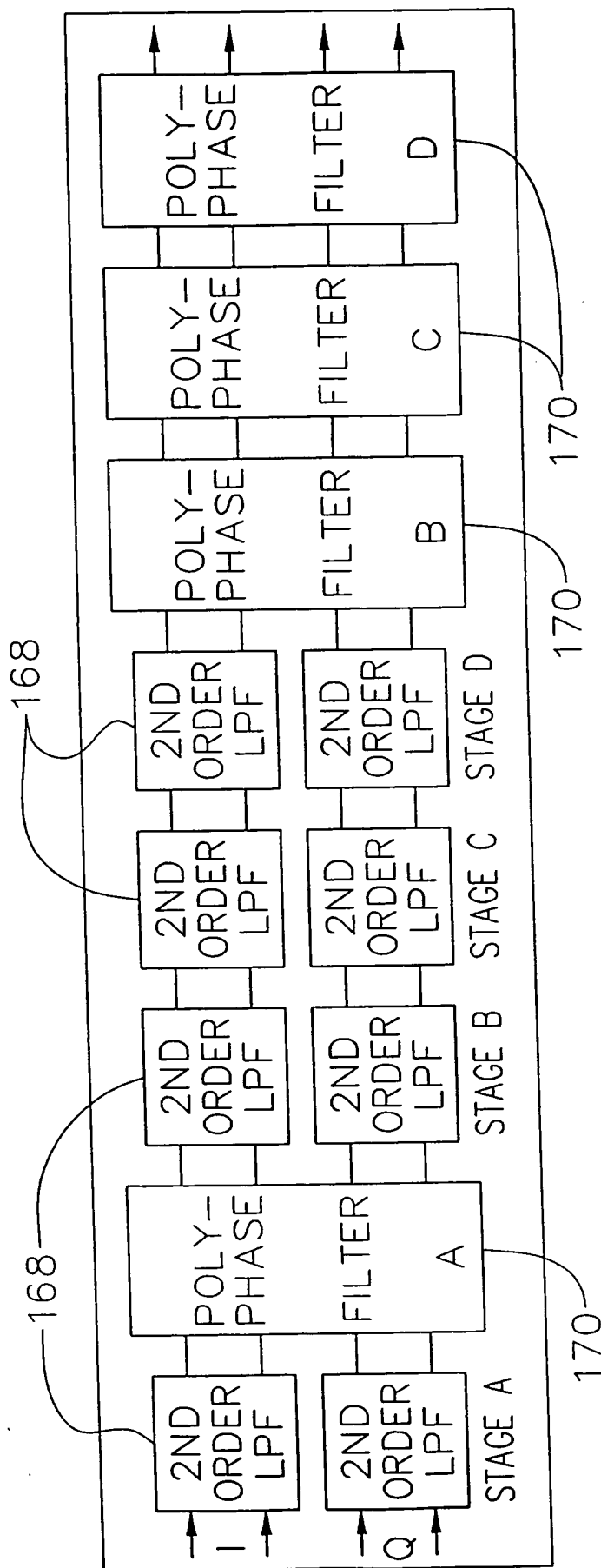
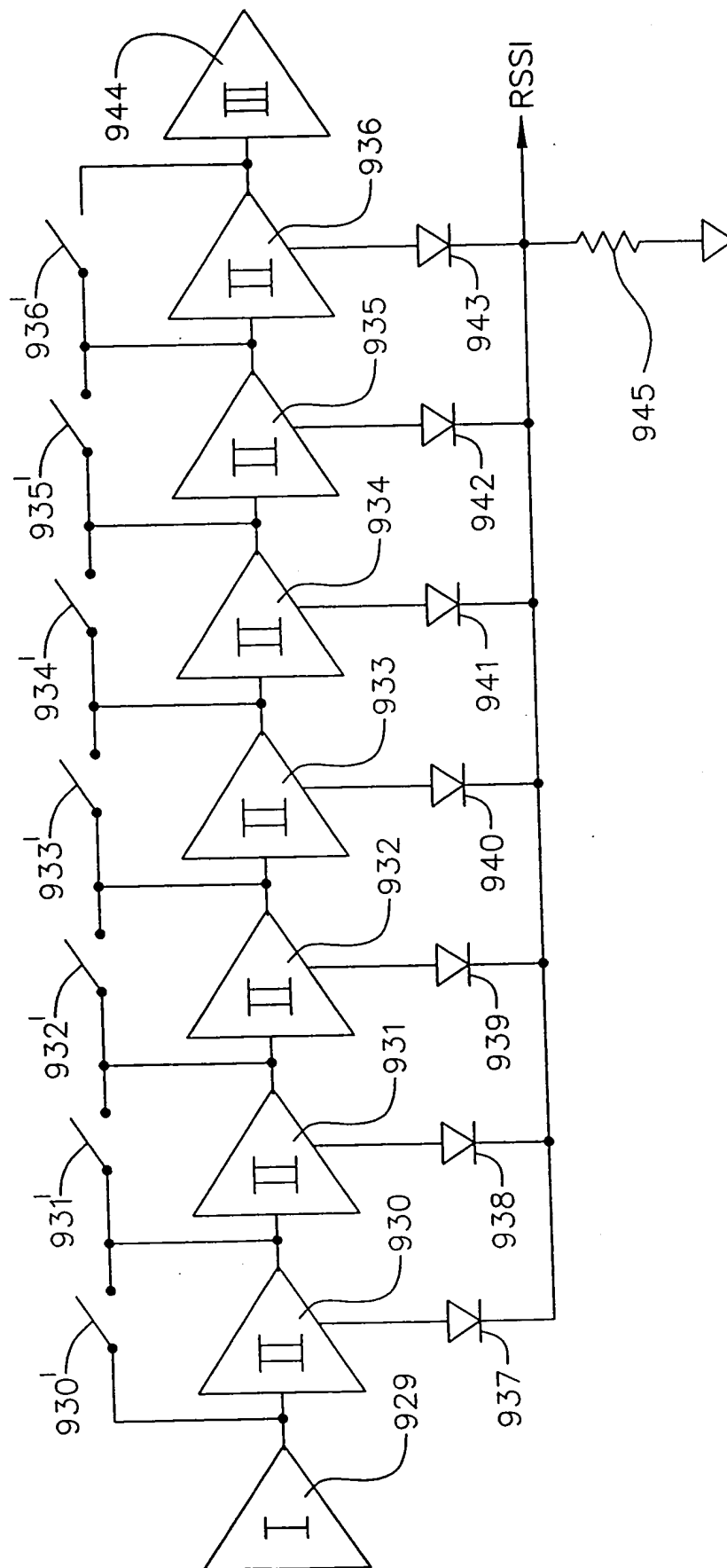




FIG. 14





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FIG. 15

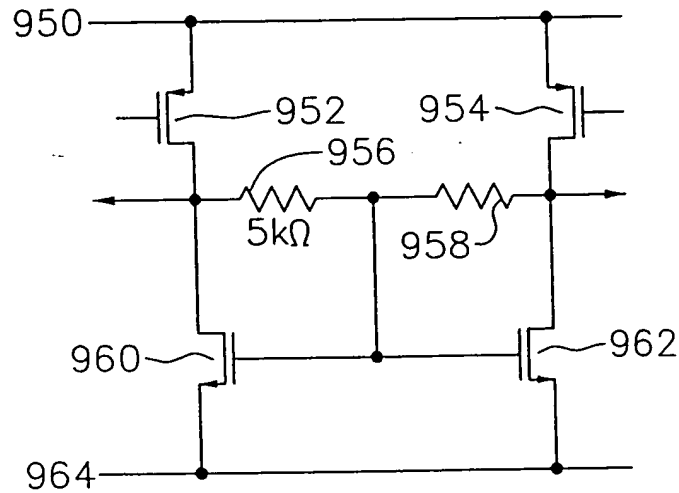
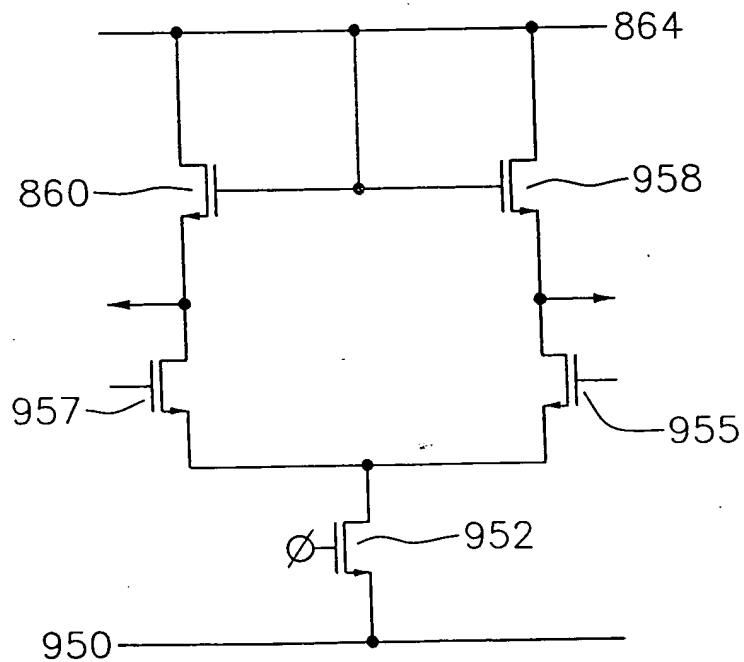


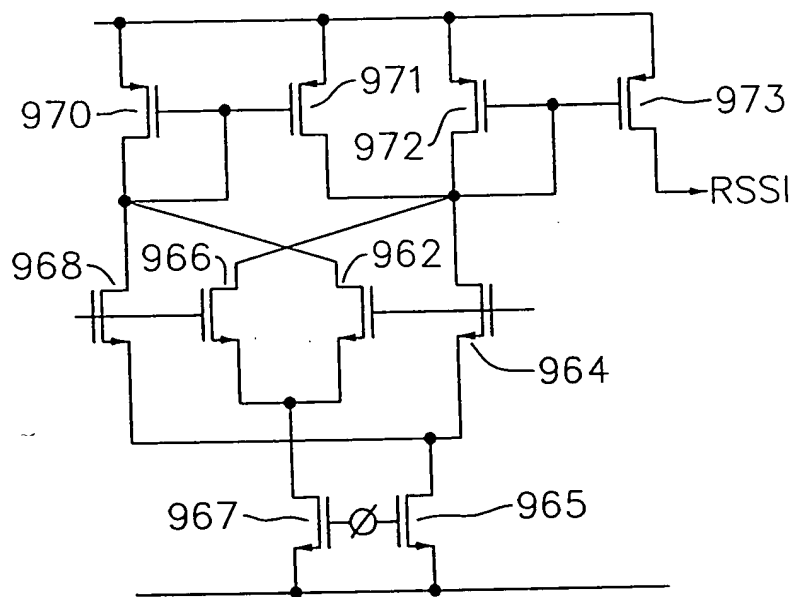
FIG. 16(α)





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FIG. 16(b)



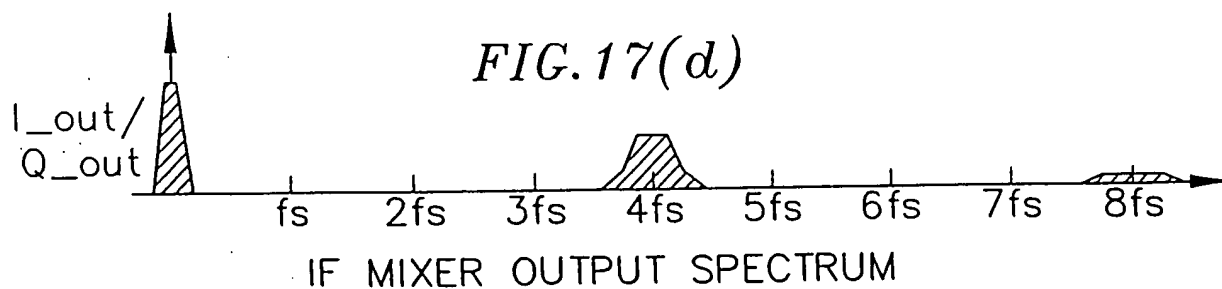
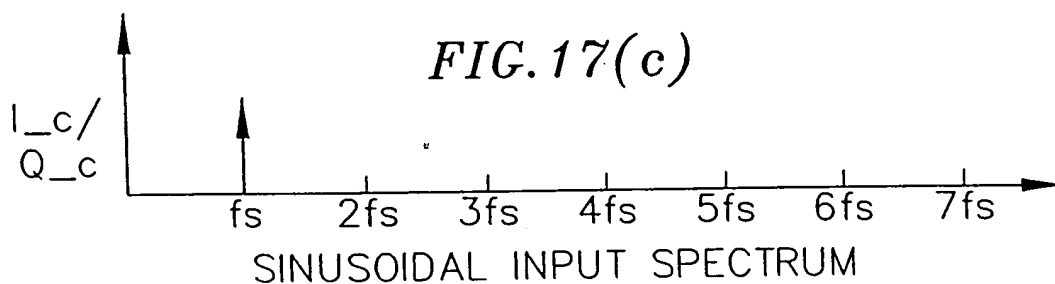
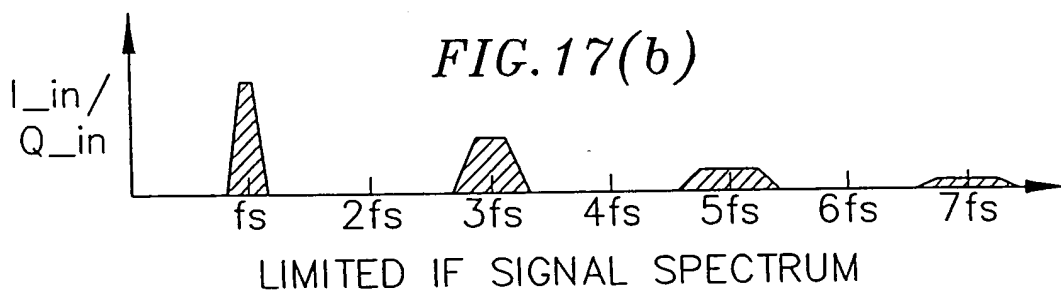
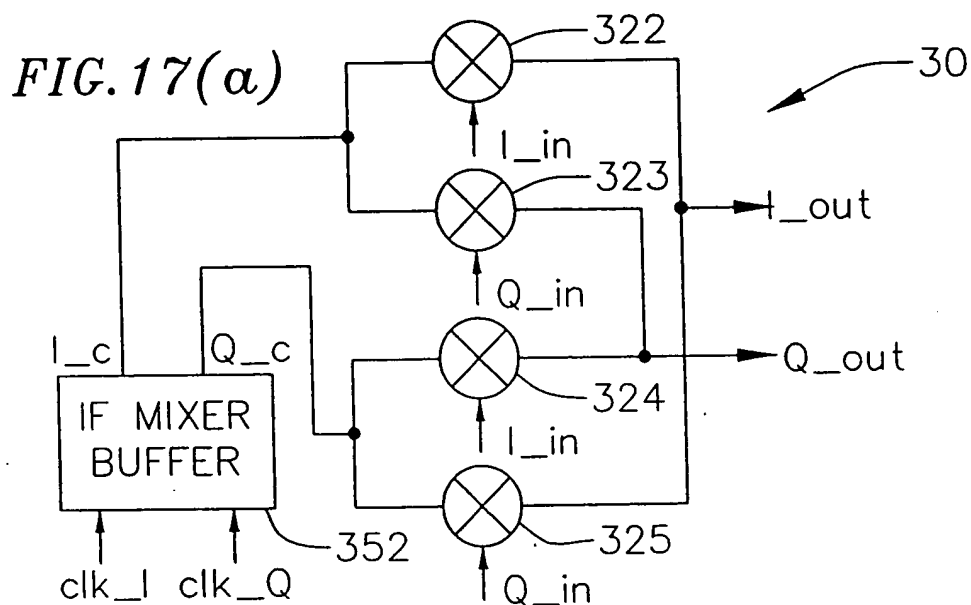




FIG. 18

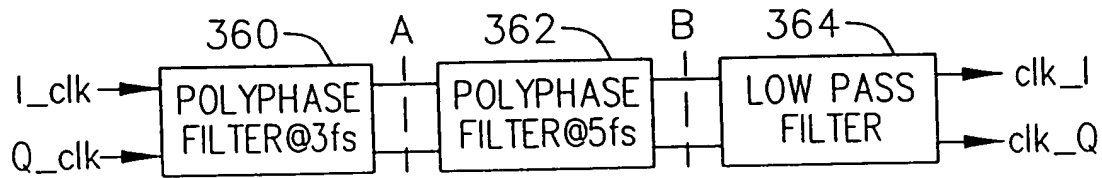


FIG. 19(a)

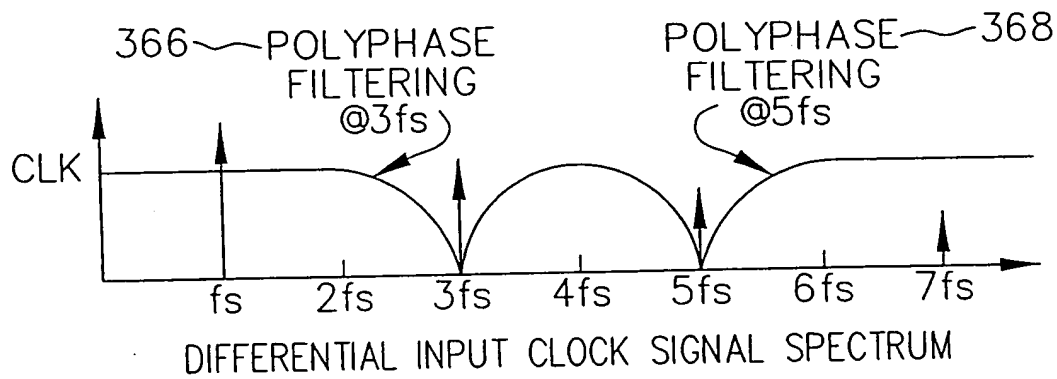


FIG. 19(b)

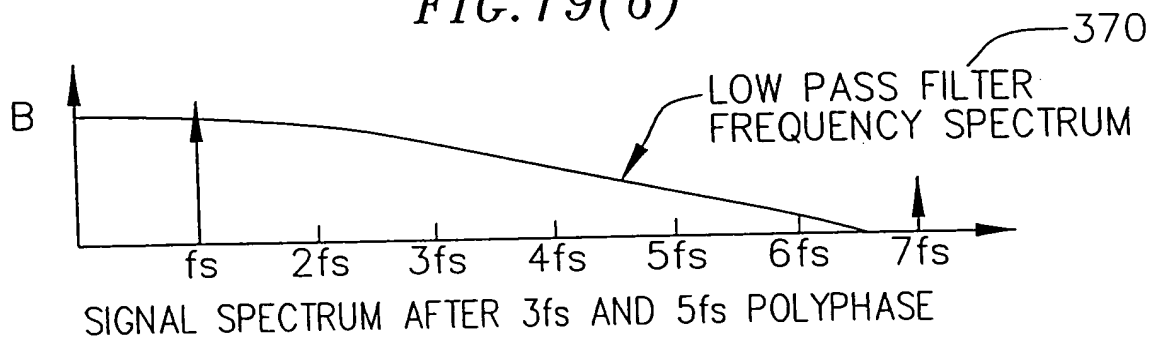


FIG. 19(c)

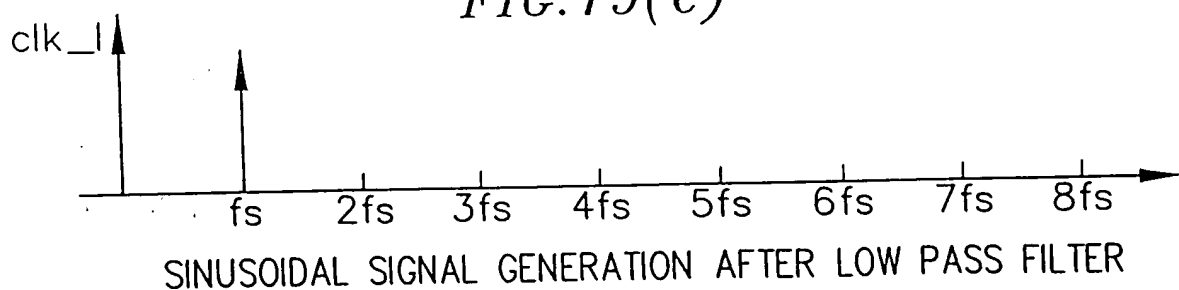




FIG.20(a)

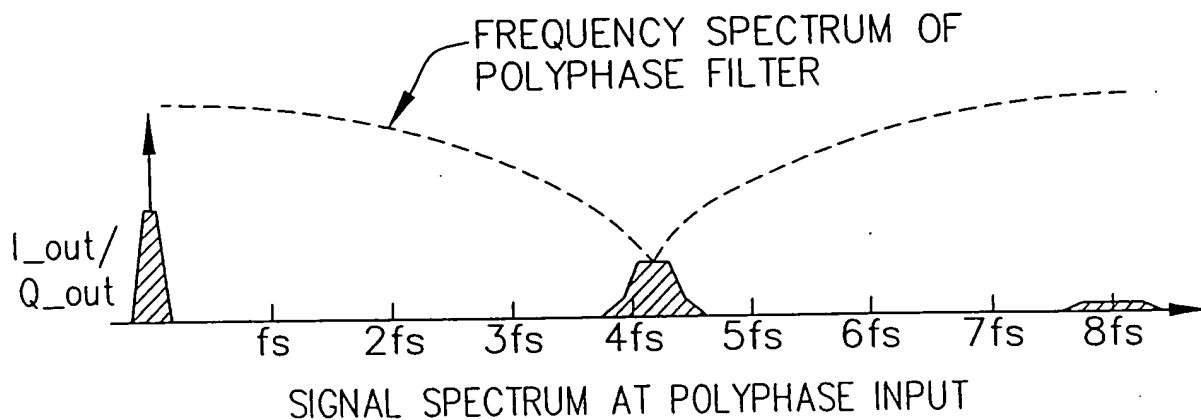


FIG.20(b)

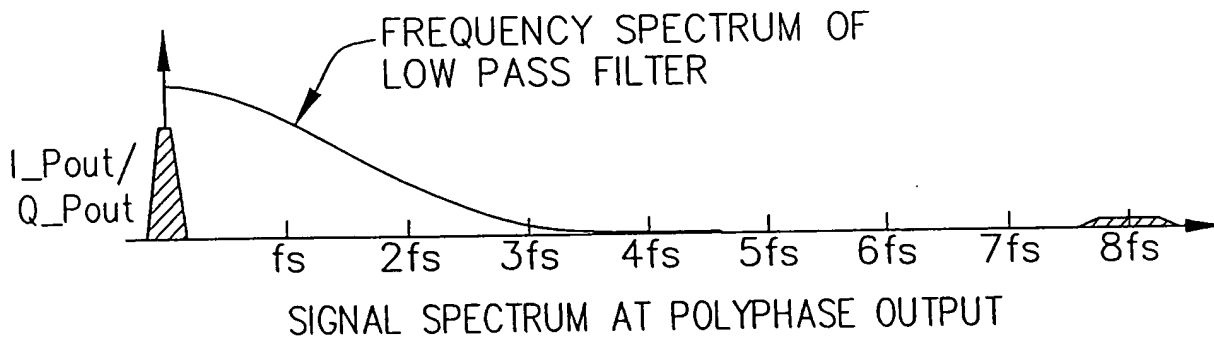
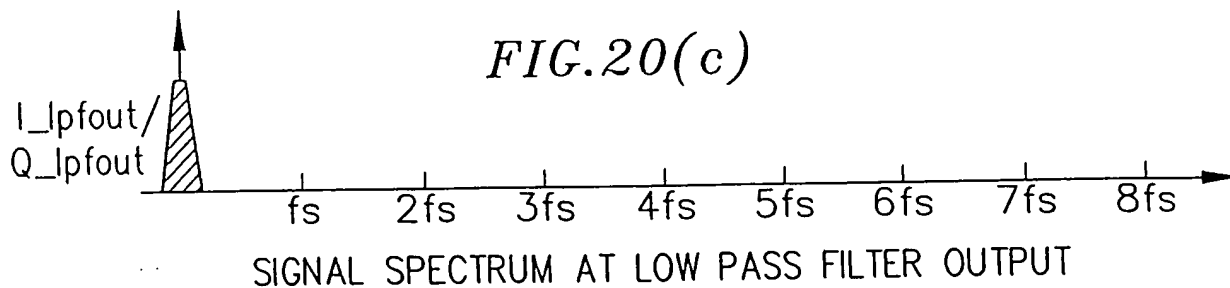


FIG.20(c)





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FIG.21

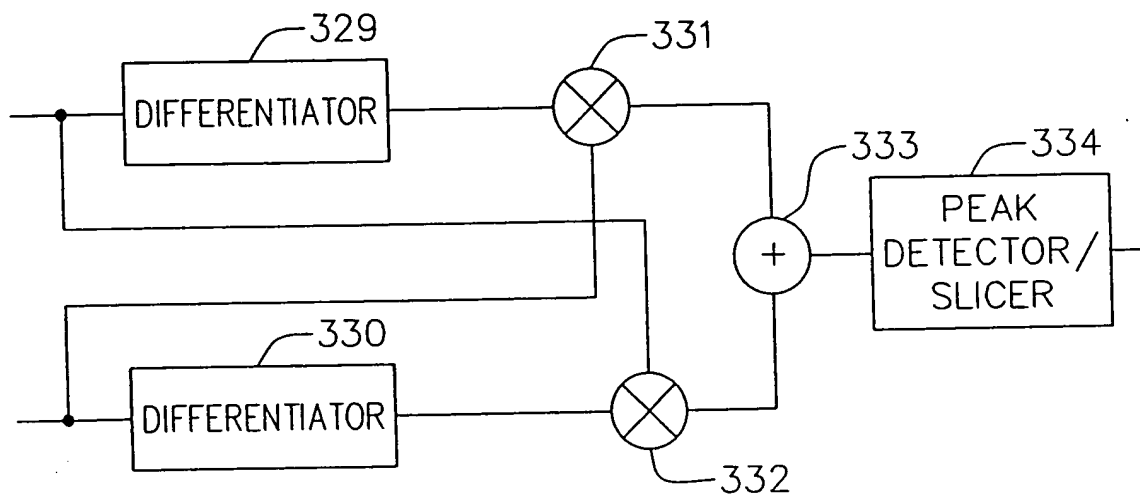
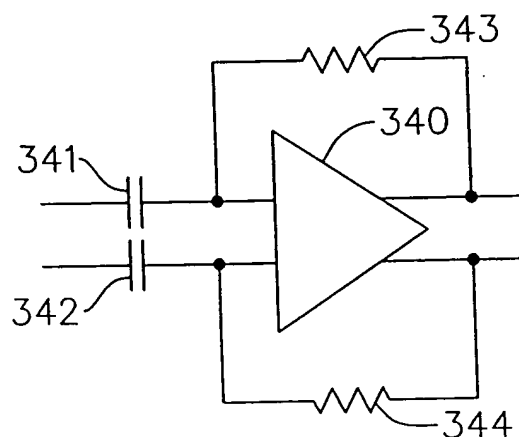
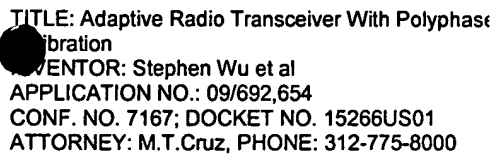


FIG.22



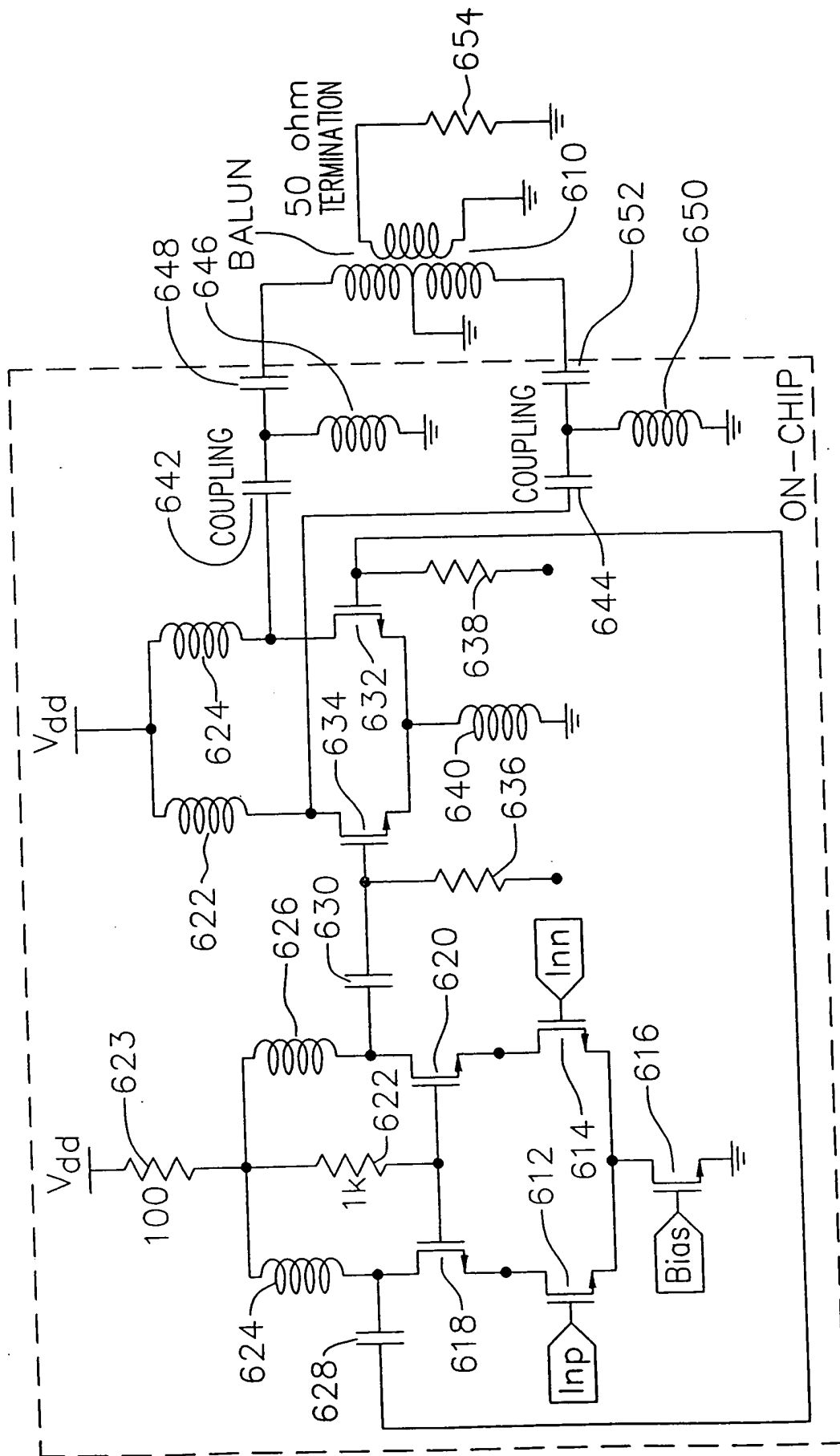


The diagram shows a differential signal processing circuit. Two input signals are fed into a differential amplifier (345). The outputs of the amplifier are connected to two inverters (350). A feedback network is connected between the outputs of the inverters and the inputs of the differential amplifier. This network consists of two resistors (348 and 349) in series, with two peak detectors (346 and 347) connected in parallel across them. The peak detectors are connected to the inputs of the differential amplifier.



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FIG. 25



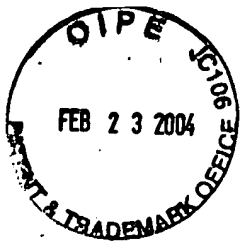


FIG.26(a)

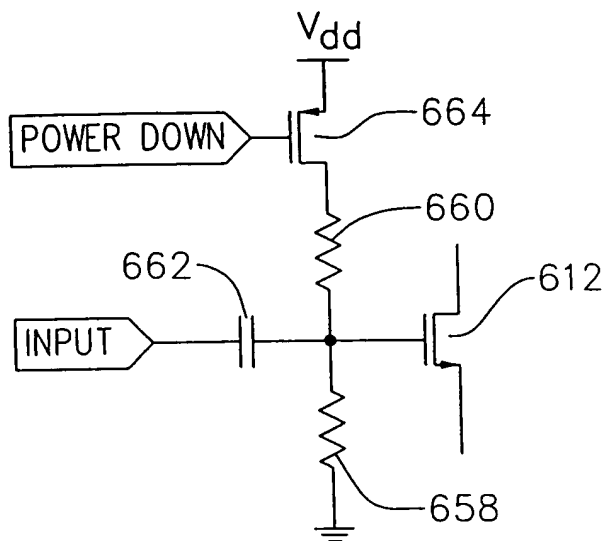


FIG.26(b)

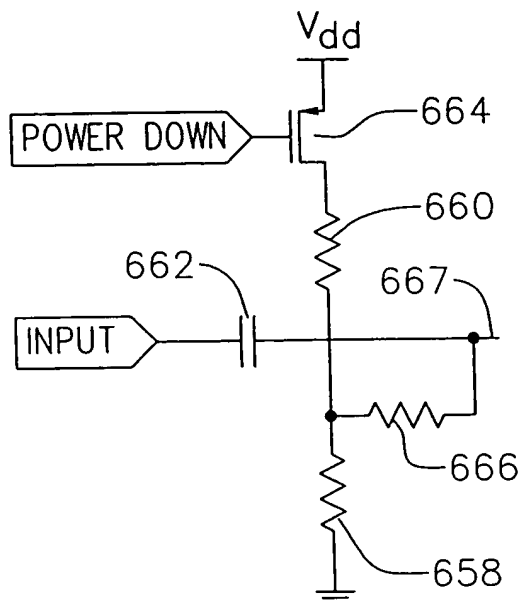


FIG.27

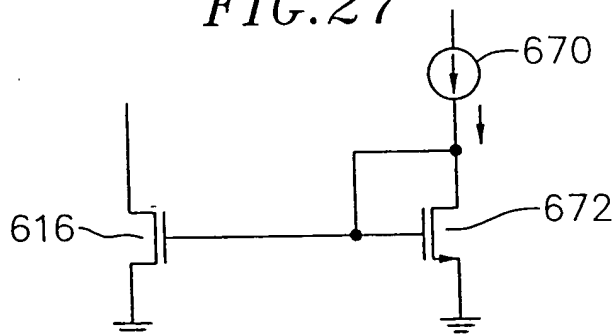
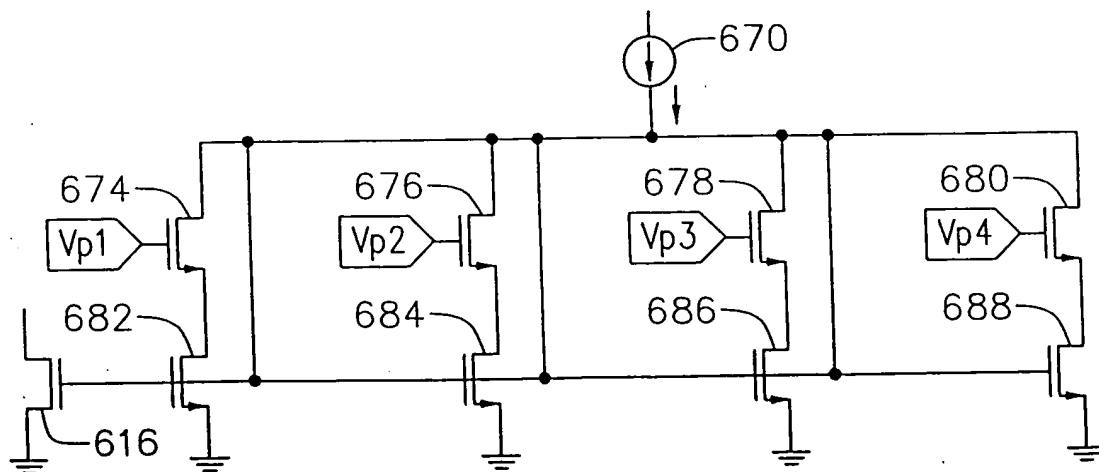


FIG.28



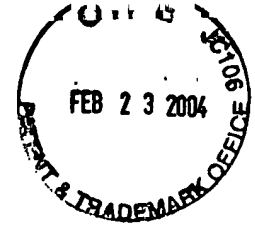


FIG.29

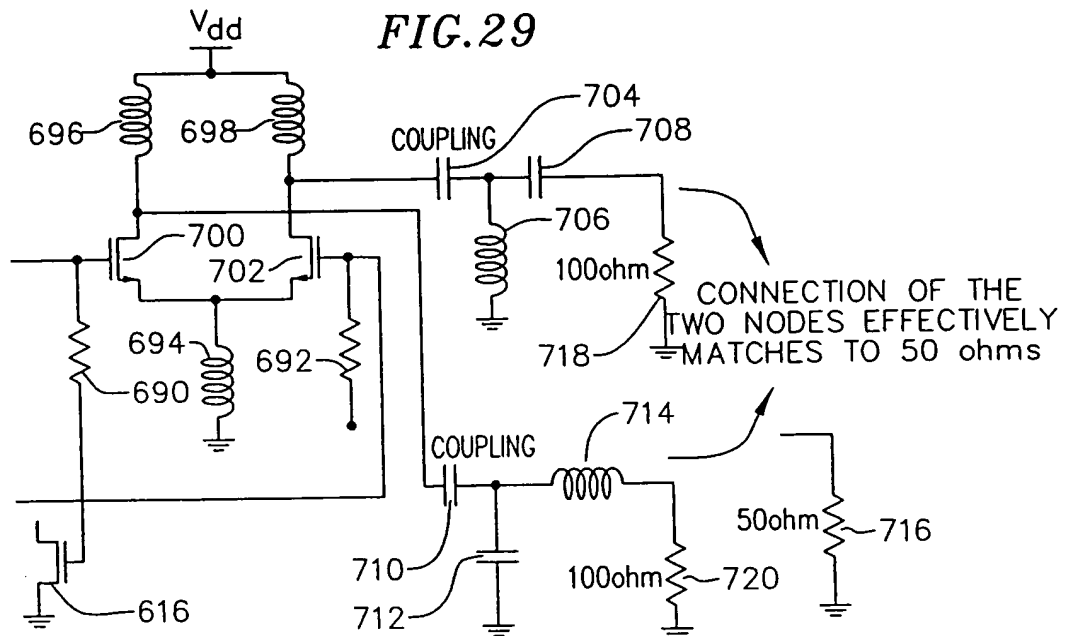
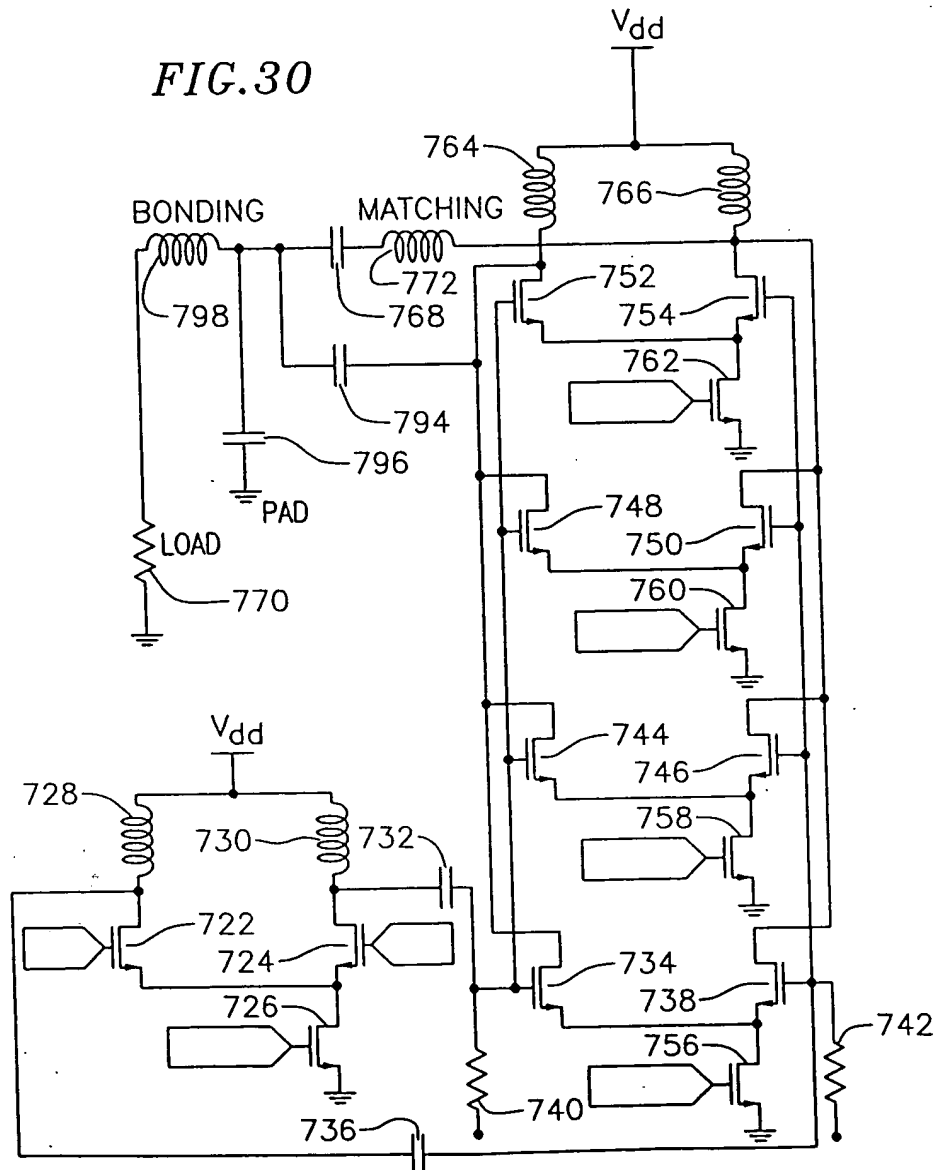
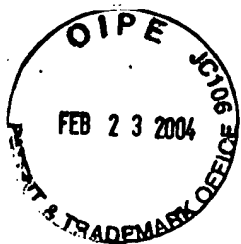


FIG.30





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FIG.31(a)

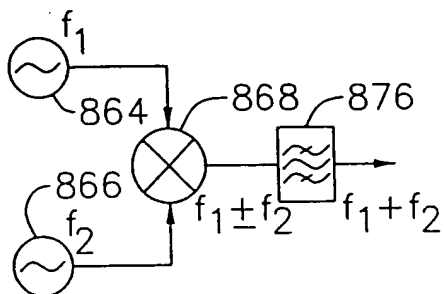


FIG.31(b)

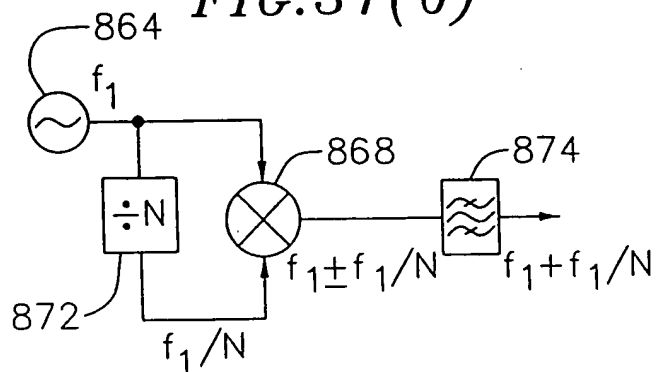


FIG.32

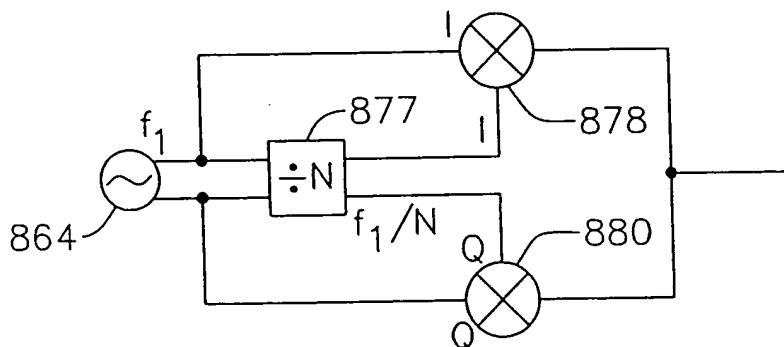


FIG.33

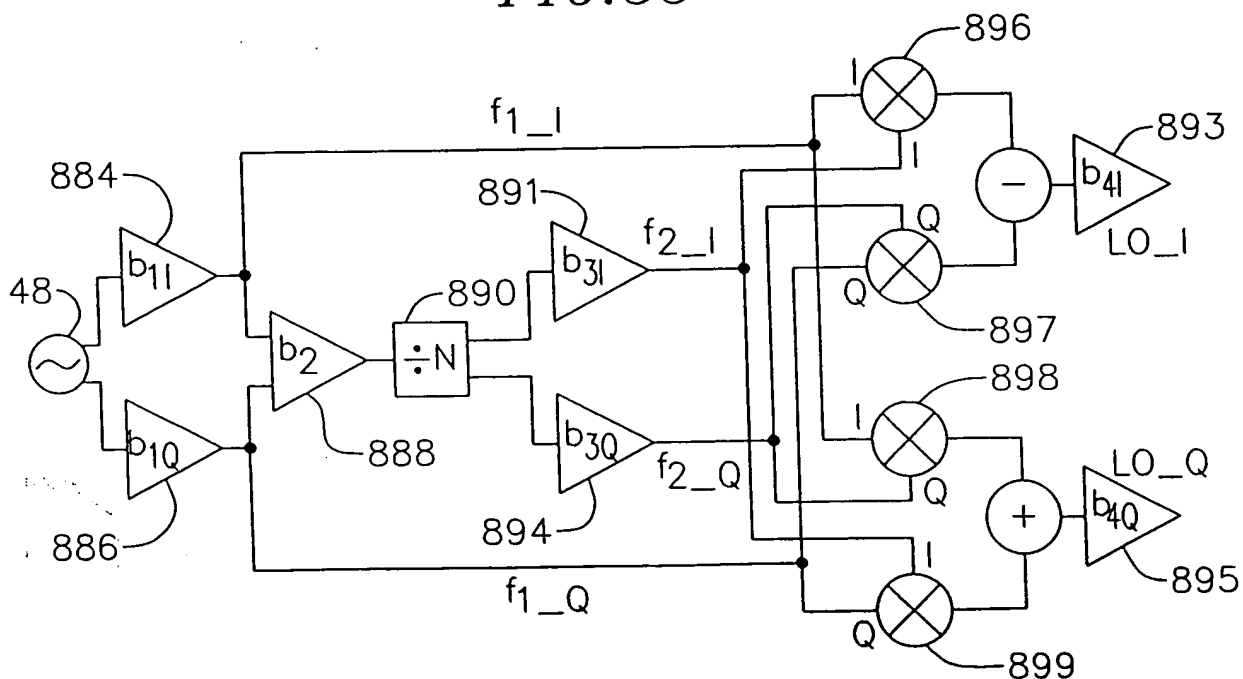




FIG.33(α)

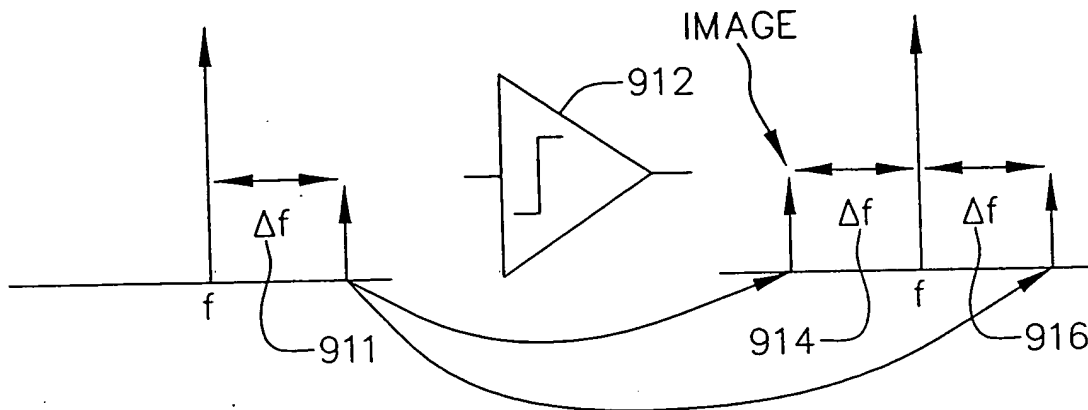
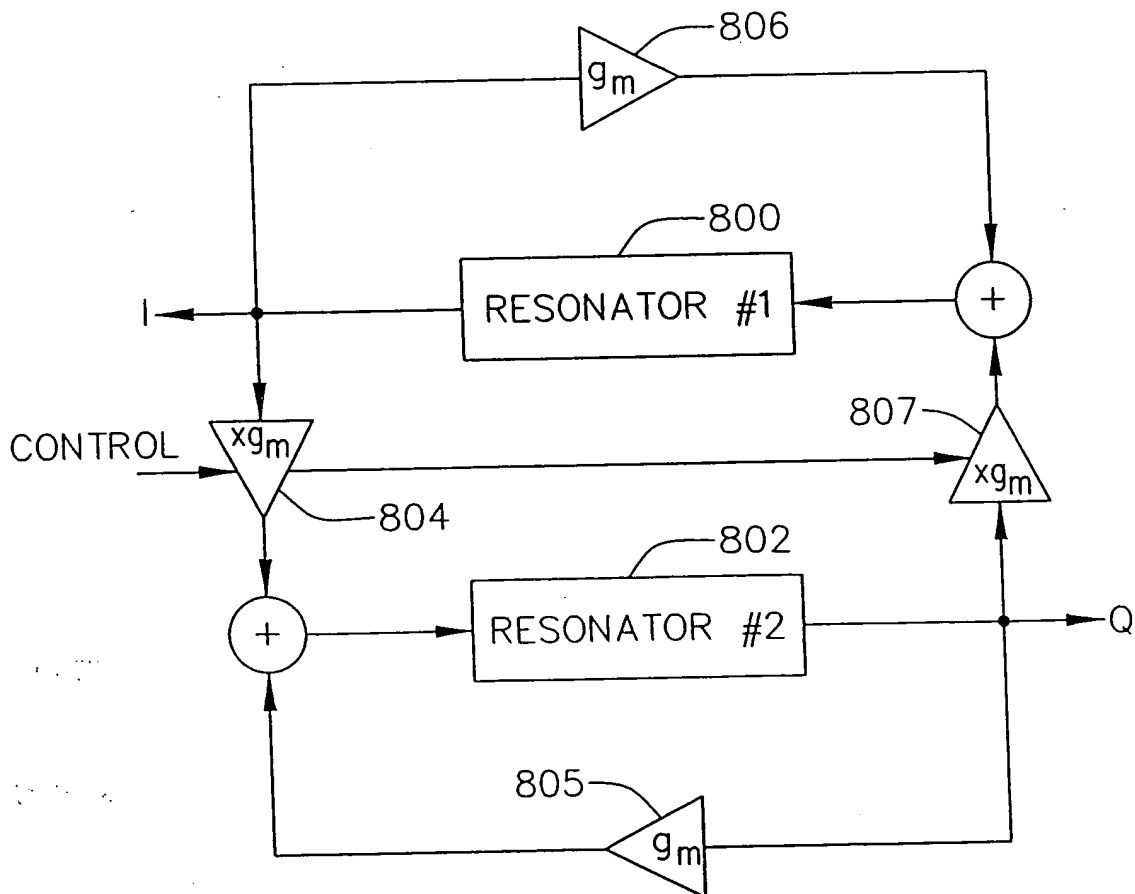


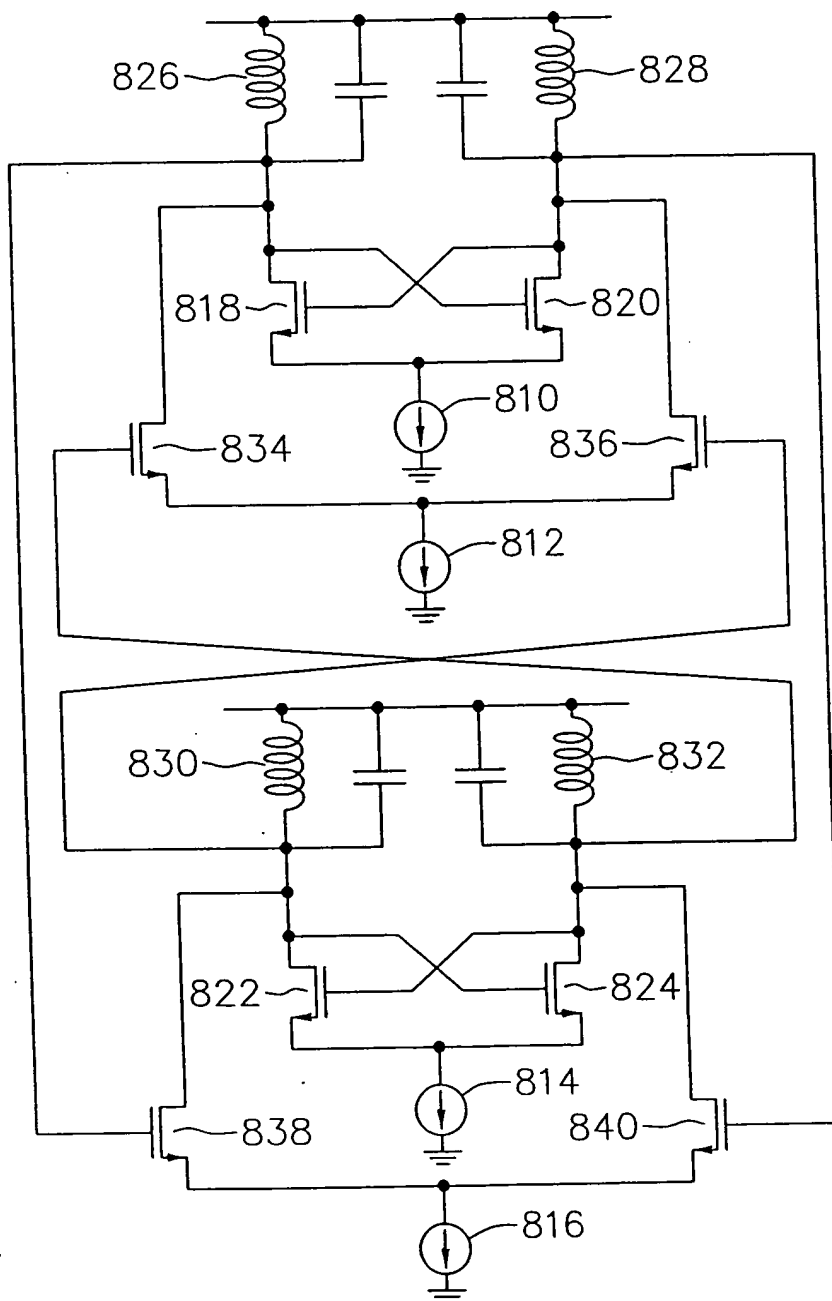
FIG.34





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FIG. 35





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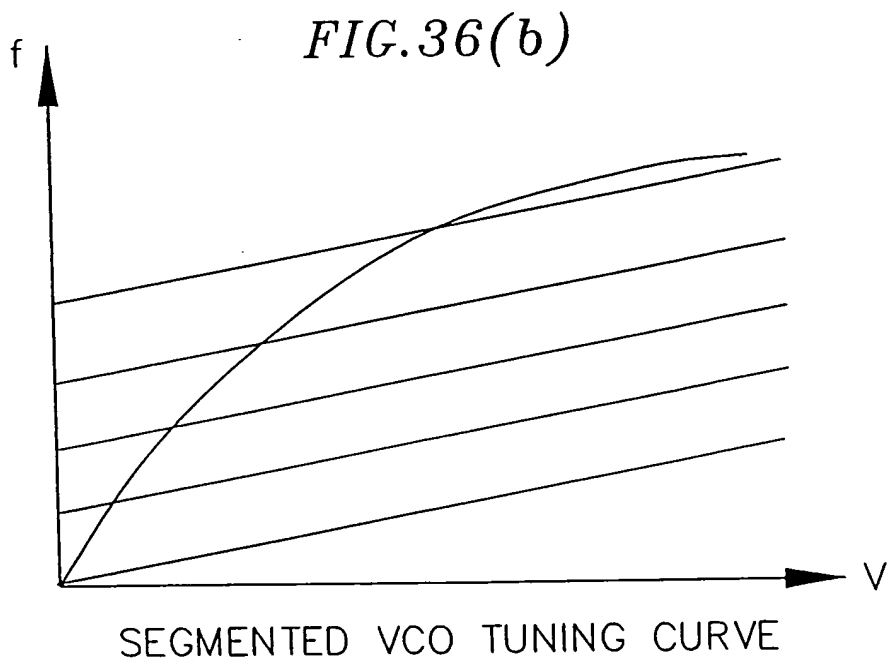
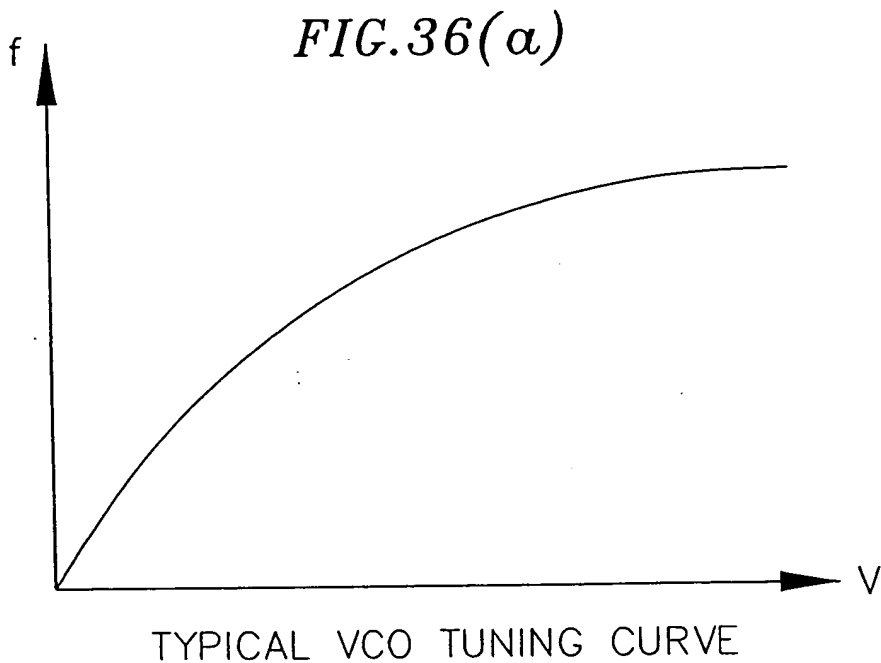




FIG.37(a)

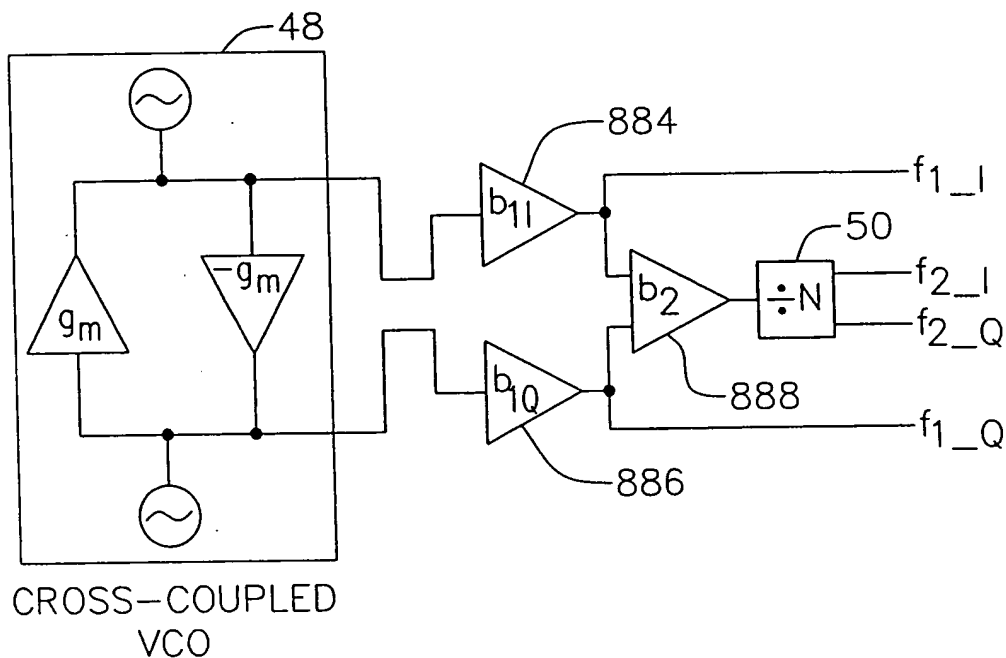


FIG.37(b)

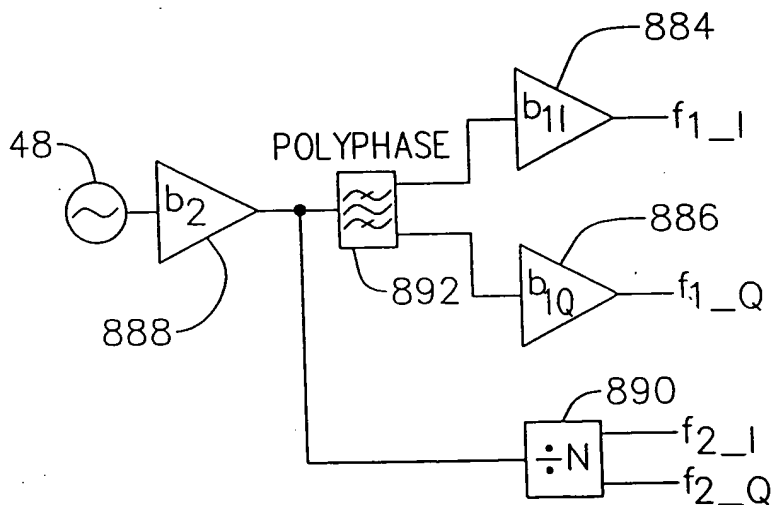
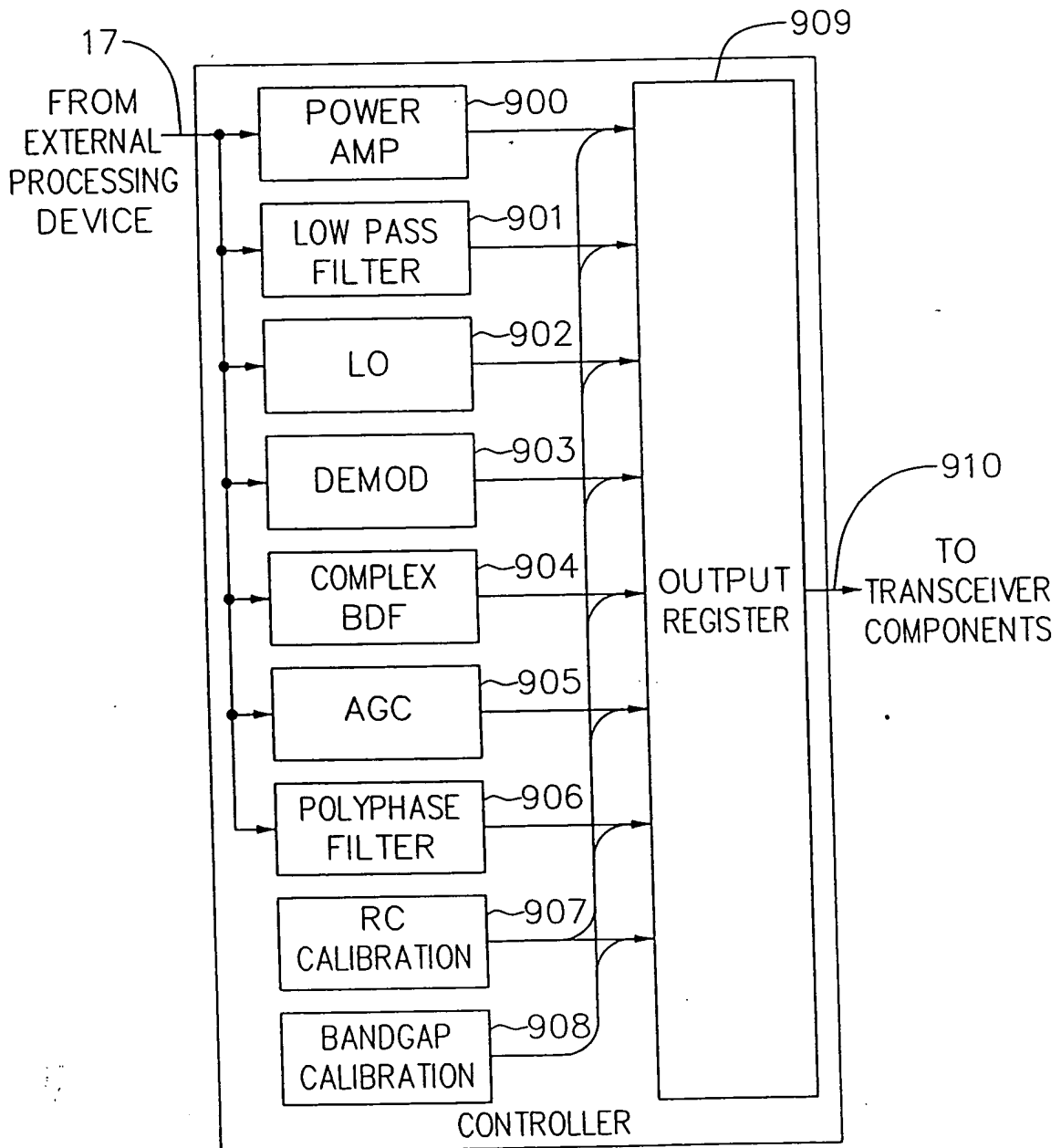




FIG.38



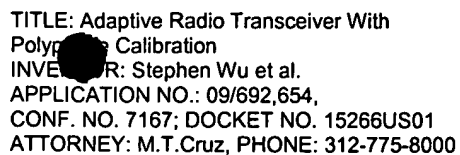


FIG. 40

The diagram illustrates a PLL (Phase-Locked Loop) circuit, labeled **FIG. 40**. The circuit includes a PLL block (280) with two polyphase outputs, **POLYPHASE A** and **POLYPHASE B**, which produce signals X_A and X_B . These signals are fed into two RSSI (Radio Signal Strength Indicator) blocks, 284 and 285. The outputs of the RSSI blocks are fed into a **CONTROL LOGIC** block (286). The **CONTROL LOGIC** block (286) is also connected to a clock input **CK (250 kHz)** and provides feedback to the PLL (280). The PLL (280) also receives inputs **I** and **Q**, and X_{IN} . The output of the **CONTROL LOGIC** block (286) is also fed back to the PLL (280). The output of the PLL (280) is also fed back to the **CONTROL LOGIC** block (286). The output of the **CONTROL LOGIC** block (286) is also fed back to the PLL (280).

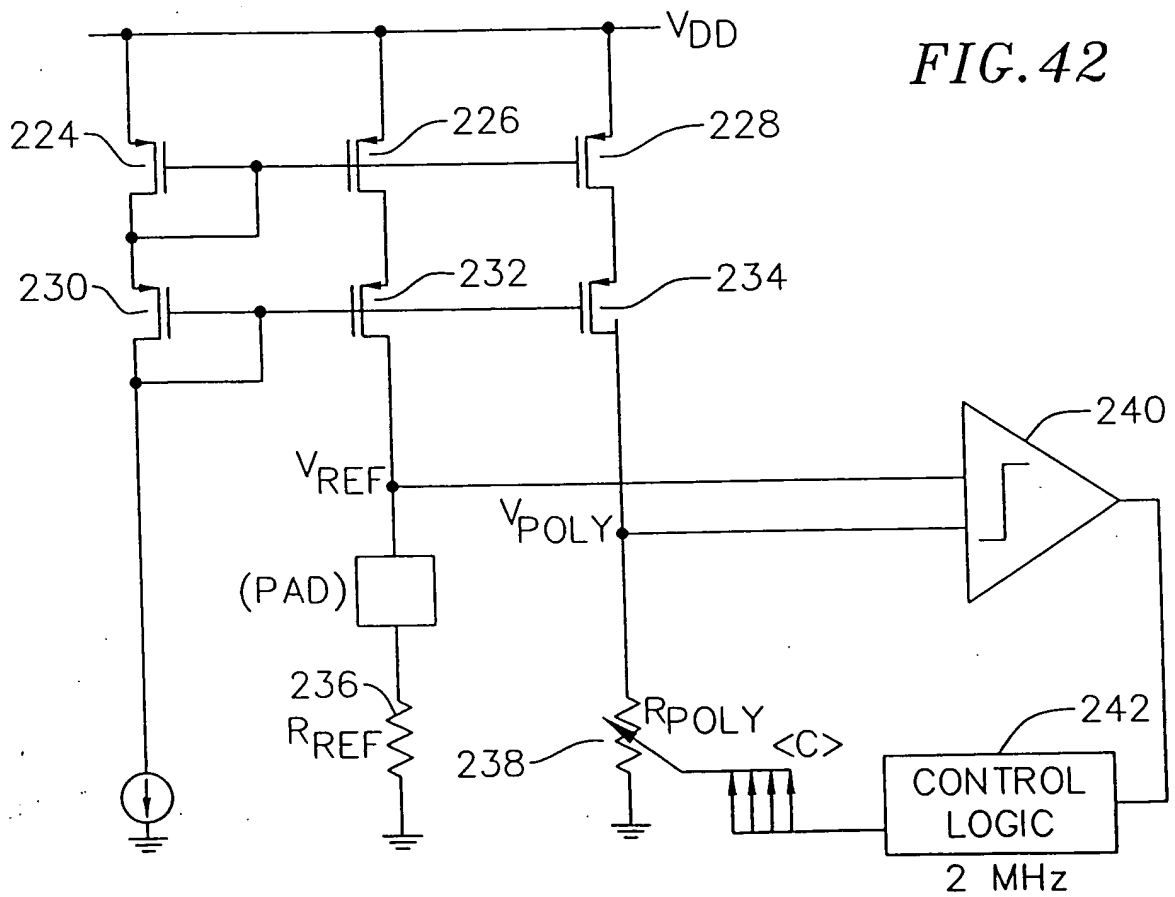
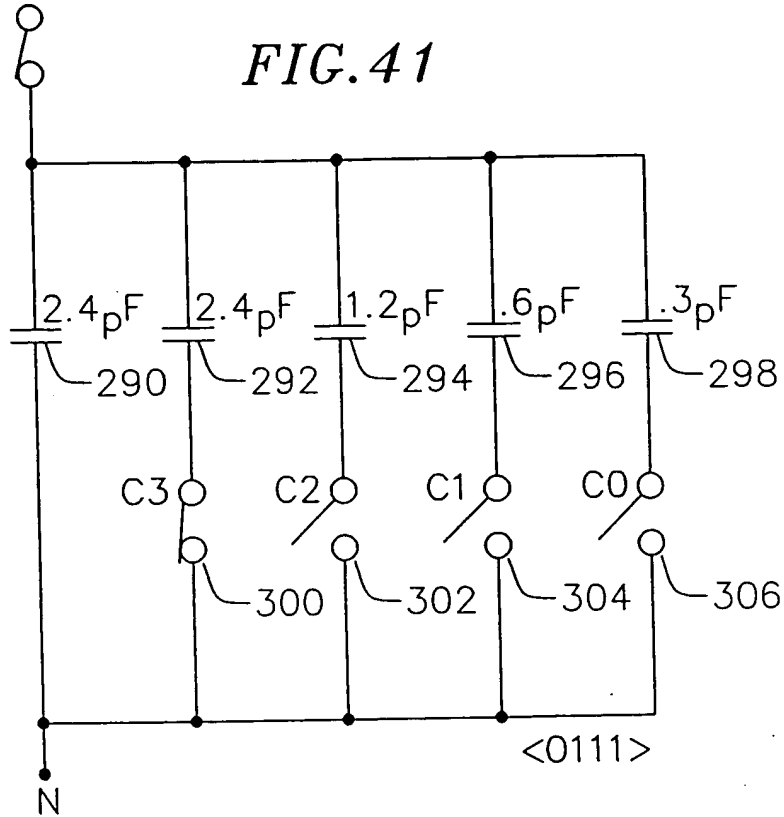




FIG. 43

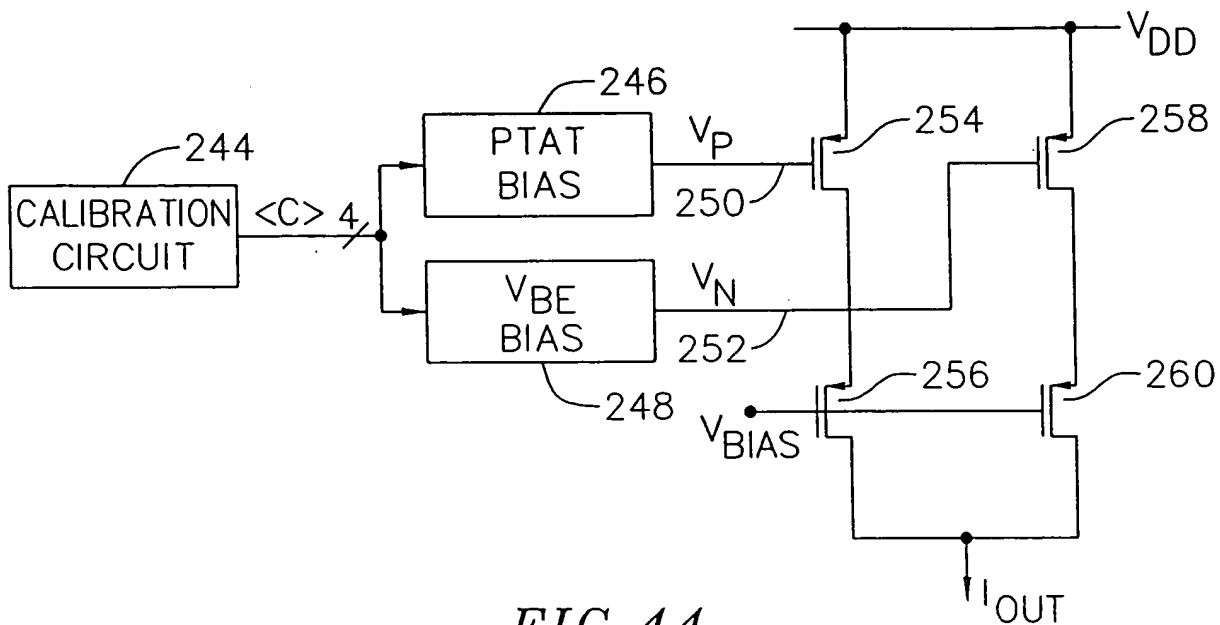


FIG. 44

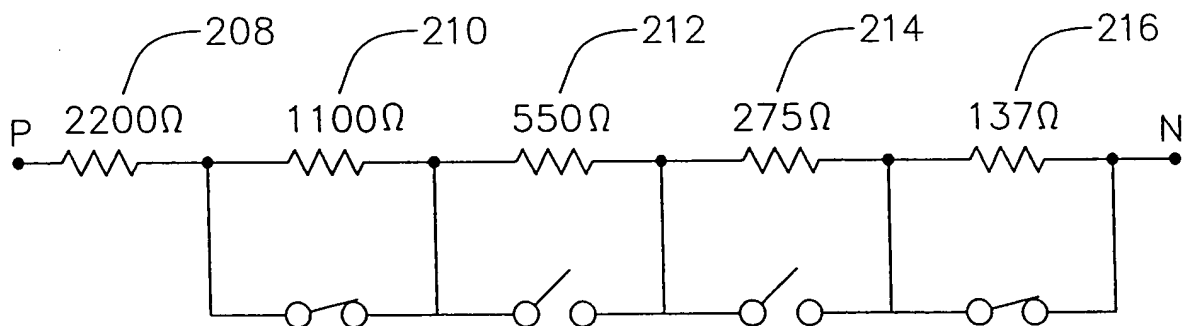


FIG. 45

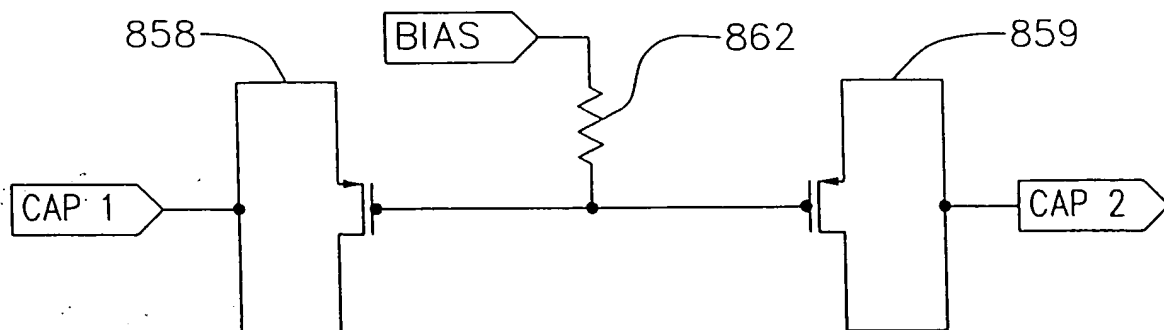




FIG. 46

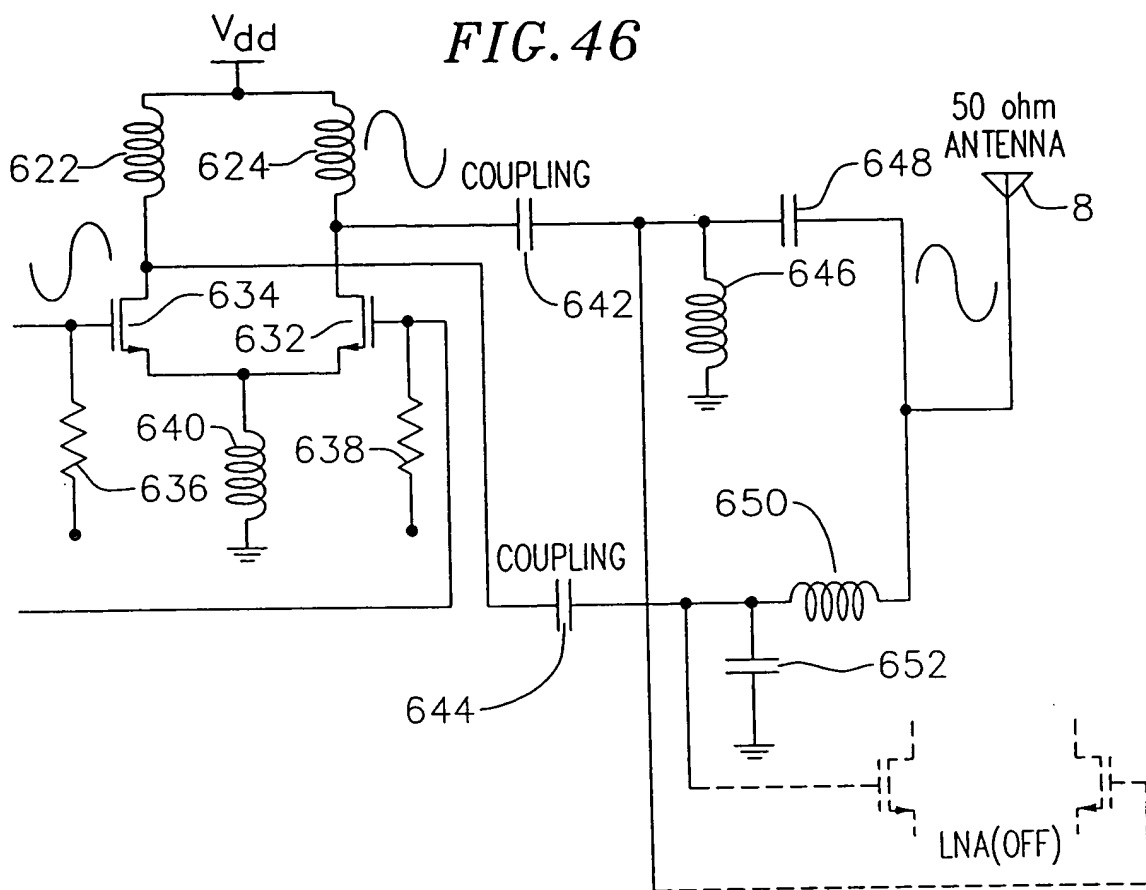


FIG. 47

